PATENT

Attorney Docket No. 125.003USR1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

James Leroy Snell

Serial No.: 10/005,483
Filed: November 9, 2001
For: HIGH DATA RATE SPREAD SPECTRUM TRANSCEIVER AND ASSOCIATED METHODS

Group Art Unit: 2631

Examiner: Not Assigned

BOX DAC
Commissioner for Patents
Washington, D.C. 20231

RENEWED PETITION UNDER 37 C.F.R. § 1.47(b) TO FILE APPLICATION WITHOUT INVENTOR'S SIGNATURE

Pursuant to 37 C.F.R. § 1.47(b), petitioner Intersil Americas Inc. ("Intersil"), respectfully seeks permission to file the above-identified reissue application without the signature of one of the inventors, James Leroy Snell. James Leroy Snell has refused to execute the reissue application. The last known address for James Leroy Snell is as follows:

	James Leroy Snell
Residence/Post Office Address:	2695 Lemon Street NE Palm Bay, FL 32905
Citizenship:	US

Snell is the inventor named on U.S. Patent No. 5,982,807, issued November 9, 1999 for "High Data Rate Spread Spectrum Transceiver and Associated Methods" (the "'807 patent").

As set forth in the Declaration of Elizabeth A. Bauer, submitted herewith, *bona fide* attempts and diligent efforts have been made to present the reissue application and corresponding inventor's declaration to James Leroy Snell for signature in accordance with MPEP 409.03(b) and 37 C.F.R. §1.47(b). As indicated in paragraphs 2 and 3 of the Declaration of David N. Fogg,

James Leroy Snell has refused to execute the reissue application and corresponding inventor's declaration.

The declaration of Paul A. Bernkopf, submitted with the prior Petition on June 28, 2002 (copy enclosed), shows that the petitioner Intersil, is the assignee of the '807 patent. Intersil filed a reissue application on the '807 patent without the inventor's signature on November 9, 2001, serial number 10/005,483, to broaden the scope of the claims of the '807 patent. Respectfully, Intersil has sufficient proprietary right to act as agent for the inventor in this application.

Filing of this reissue application is necessary to preserve the rights of the parties hereto. Irreparable harm will result to Intersil if the petition is not granted as shown by the Declaration of Paul A. Bernkopf.

Applicant previously submitted a Reissue Application: Consent of Assignee: Statement of Non-Assignment and Statement under 37 C.F.R. 3.73(b) (copies enclosed) on June 28, 2002.

It is Applicant's understanding that there are no additional fees for this RENEWED Petition. However, if any additional fees or credits are deemed necessary, please charge or credit Deposit Account No. 502432

Based on the foregoing, it is respectfully submitted that the petitioner has demonstrated sufficient proprietary interest to make the reissue application on behalf of and as agent for the inventor James Leroy Snell who has refused to sign the inventor declaration. Petitioner respectfully requests that the petition Under 37 CFR §1.47(b) be granted.

Respectfully submitted,

Date: November 27, 2002

David N. Fogg
Reg. No. 35,138

Attorneys for Applicant
Fogg & Associates, LLC
P.O. Box 581339
Minneapolis, MN 55458-1339
Telephone: 612-332-4720
Facsimile: 612-677-3553

Declaration Of Paul A. Bernkopf

I, Paul A. Bernkopf, hereby declare:

1. I am Chief Intellectual Property Counsel and Corporate Vice President of Intersil Americas Inc., formerly known as Intersil Corporation and Intersil Communications Inc. ("Intersil"). Intersil is a successor in interest to Harris Corporation and assignee of Harris Corporation's interest in certain intellectual property, including U.S. Patent No. 5,982,807, issued to James Leroy Snell, inventor, on November 9, 1999 for "High Data Rate Spread Spectrum Transceiver And Associated Methods" (the "'807 patent"), as shown by assignment dated August 11, 1997, and recorded on September 19, 1997, at Reel: 8728, Frame: 0769, in the United States Patent and Trademark Office.

2. James Leroy Snell is a former employee of Harris Corporation and Intersil. He was involved in research and development of Harris Corporation and Intersil products. Snell is sole inventor of the "'807 patent." On information and belief, he is retired.

3. James Leroy Snell agreed in writing to assign all of his right, title and interest in and to the invention of the '807 patent to Harris Corporation, Intersil's predecessor in interest, as shown by assignment dated August 11, 1997, and recorded on September 19, 1997, at Reel: 8728, Frame: 0769, in the United States Patent and Trademark Office.

4. Intersil filed a reissue application on the '807 patent without the inventor's signature on November 9, 2001, RE 10/005,483, to broaden the scope of the claims of the '807 patent.

5. The invention of the '807 patent represents valueable intellectual property of Intersil. Intersil will be irreparably harmed if it is not able to exploit this intellecual property by filing and prosecuting the subject reissue application since the scope of the invention was not fully realized by the claims of of the '807 patent.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Paul A. Bernkopf
Dated: 6/26/02

PTO/SB/53 (10-00)
Approved for use through 12/30/2000. OMB 0651-0033
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

REISSUE APPLICATION: CONSENT OF ASSIGNEE; STATEMENT OF NON-ASSIGNMENT

Docket Number (Optional): 125.003USR1

This is part of the application for a reissue patent based on the original patent identified below.

Name of Patentee(s): James Leroy Snell

Patent Number	Date Patent Issued
5,982,807	November 9, 1999

Title of Invention:
HIGH DATA RATE SPREAD SPECTRUM TRANSCEIVER AND ASSOCIATED METHODS

1. [X] Filed herein is a certificate under 37 CFR 3.73(b). (Form PTO/SB/96)

2. [ ] Ownership of the patent is in the inventor(s), and no assignment of the patent is in effect.

One of boxes 1 or 2 above must be checked. If multiple assignees, complete this form for each assignee. If box 2 is checked, skip the next entry and go directly to "Name of Assignee".

The written consent of all assignees and inventors owning an undivided interest in the original patent is included in this application for reissue.

The assignee(s) owning an undivided interest in said original patent is/are Intersil Americas, Inc., 7585 Irvine Center Drive, Suite 100, Irvine, California 92618, and the assignee(s) consents to the accompanying application for reissue.

Name of assignee/inventor (if not assigned)

Signature: Paul A. Bernkopf

Date: 6/26/02

Typed or printed name and the title of person signing for assignee (if assigned)

Paul A. Bernkopf
Chief Intellectual Property Counsel & Corporate Vice President

PTO/SB/96 (6-98)
Approved for use through 09/30/2000. OMB 0651-0031
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Intersil Americas, Inc.

Application No./Patent No.: 08/819,846 - 5,982,807 Filed/Issue Date: 03/17/97 - 11/09/99

Entitled: HIGH DATA RATE SPREAD SPECTRUM TRANSCEIVER AND ASSOCIATED METHODS

Intersil Americas Inc. (Name of Assignee), a corporation (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.),

states that it is:

1. ☑ the assignee of the entire right, title, and interest; or
2. ☐ an assignee of an undivided part interest

in the patent application/patent identified above by virtue of either:

A. [ ] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

OR

B. [✓] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as shown below:

1. From: James Leroy Snell To: Harris Corporation
   The document was recorded in the Patent and Trademark Office at
   Reel 8728, Frame 0769, or for which a copy thereof is attached.
2. From: Harris Corporation To: Intersil Corporation
   The document was recorded in the Patent and Trademark Office at
   Reel 10884, Frame 0394, or for which a copy thereof is attached.
3. From: Intersil Corporation To: Intersil Communication Inc.
   The document was recorded in the Patent and Trademark Office at
   Reel _____, Frame _____, or for which a copy thereof is attached.

[✓] Additional documents in the chain of title are listed on a supplemental sheet.

[✓] Copies of assignments or other documents in the chain of title are attached.
[NOTE: A separate copy (*i.e.*, the original assignment document or a true copy of the original document) must be submitted to Assignment Division in accordance with 37 CFR Part 3, if the assignment is to be recorded in the records of the PTO. See MPEP 302-302.8]

The undersigned (whose title is supplied below) is empowered to sign this statement on behalf of the assignee.

6/26/02
Date

Signature

Paul A. Bernkopf
Typed or printed name

Chief IP Counsel & Corporate VP
Title

4. From: Intersil Communication Inc.
To: Intersil Americas Inc.
This document is attached, but has not been recorded in the U.S. Patent and Trademark Office.

State of Delaware

Office of the Secretary of State

I, HARRIET SMITH WINDSOR, SECRETARY OF STATE OF THE STATE OF DELAWARE, DO HEREBY CERTIFY THE ATTACHED IS A TRUE AND CORRECT COPY OF THE RESTATED CERTIFICATE OF "INTERSIL CORPORATION", CHANGING ITS NAME FROM "INTERSIL CORPORATION" TO "INTERSIL COMMUNICATIONS, INC.", FILED IN THIS OFFICE ON THE TWENTY-FIFTH DAY OF MAY, A.D. 2001, AT 4:15 O'CLOCK P.M.

A FILED COPY OF THIS CERTIFICATE HAS BEEN FORWARDED TO THE NEW CASTLE COUNTY RECORDER OF DEEDS.

Harriet Smith Windsor

Harriet Smith Windsor, Secretary of State

AUTHENTICATION: 1155634

DATE: 05-25-01

3050122 8100

010253080

AMENDED AND RESTATED CERTIFICATE OF INCORPORATION
OF
INTERSIL CORPORATION

INTERSIL CORPORATION, a corporation organized and existing under the laws of the State of Delaware, hereby certifies as follows:

FIRST: The present name of the corporation is INTERSIL CORPORATION and the name under which the corporation was originally incorporated is HSS Operating Corporation. The date of filing of its original Certificate of Incorporation with the Secretary of State of the State of Delaware was June 2, 1999.

SECOND: This Amended and Restated Certificate of Incorporation (the "Certificate") restates and integrates and further amends in its entirety the Certificate of Incorporation of this corporation. This Certificate was duly adopted by a majority vote of the stockholders of the corporation in accordance with Sections 228, 242 and 245 of the General Corporation Law of the State of Delaware.

THIRD: This Certificate shall become effective immediately upon its filing with the Secretary of State of the State of Delaware.

FOURTH: Upon the filing of the Certificate with the Secretary of State of the State of Delaware, the Certificate of Incorporation of the corporation shall be amended and restated in its entirety to read as set forth on Exhibit A attached hereto.

IN WITNESS WHEREOF, said corporation has caused this Certificate to be executed by a duly authorized officer this 23rd day of May, 2001.

By: _____
Gregory Williams
Chief Executive Officer

STATE OF DELAWARE
SECRETARY OF STATE
DIVISION OF CORPORATIONS
FILED 04:15 PM 05/25/2001
010253080 – 3050122

EXHIBIT A

AMENDED AND RESTATED CERTIFICATE OF INCORPORATION

OF

INTERSIL COMMUNICATIONS, INC.

1. *Name.* The name of the Corporation is Intersil Communications, Inc.

2. *Registered Office and Agent.* The address of the Corporation's registered office in the State of Delaware is 1209 Orange Street, in the City of Wilmington, County of New Castle. The name of the Corporation's registered agent at such address is The Corporation Trust Company.

3. *Purpose.* The purposes for which the Corporation is formed are to engage in any lawful act or activity, including, without limitation, forming and/or acquiring foreign subsidiaries, for which corporations may be organized under the General Corporation Law of the State of Delaware ("DGCL") and to possess and exercise all of the powers and privileges granted by such law and any other law of Delaware.

4. *Authorized Capital.* The aggregate number of shares of stock which the Corporation shall have authority to issue is One Thousand (1,000) shares, all of which are of one class and are designated as Common Stock, par value $.01 per share.

5. *Incorporator.* The name and mailing address of the incorporator are Marian T. Ryan, 4000 Bell Atlantic Tower, 1717 Arch Street, Philadelphia, Pennsylvania 19103-2793.

6. *Bylaws.* In furtherance and not in limitation of the powers conferred by law, the board of directors of the Corporation is authorized to adopt, amend or repeal the bylaws of the Corporation, except as otherwise specifically provided therein, subject to the powers of the stockholders of the Corporation to amend or repeal any bylaws adopted by the board of directors.

7. *Elections of Directors.* Elections of directors need not be by written ballot unless and except to the extent the bylaws of the Corporation shall so provide.

8. *Right to Amend.* The corporation reserves the right to amend or repeal any provision contained in this Certificate as the same may from time to time be in effect in the manner now or hereafter prescribed by law, and all rights, preferences and privileges conferred on stockholders, director or others hereunder are subject to such reservation.

9. *Unanimous Written Consent Required.* If any action is to be taken by stockholders without a meeting, such action must be authorized by unanimous written consent signed by all of the holders of outstanding voting stock.

10. *Limitation on Liability.* The directors of the Corporation shall be entitled to the benefits of all limitations on the liability of directors generally that are now or hereafter become available under the DGCL. Without limiting the generality of the foregoing, to the fullest extent permitted by the DGCL, as it exists on the date hereof or as it may hereafter be amended, no director of the Corporation shall be personally liable to the Corporation or its stockholders for monetary damages for breach of fiduciary duty as a director, except for liability (i) for any breach of the director's duty of loyalty to the Corporation or its stockholders, (ii) for acts or omissions not in good faith or which involve intentional misconduct or a knowing violation of law, (iii) under Section 174 of the DGCL, or (iv) for any transaction from which the director derived an improper personal benefit. Any repeal or modification of this Section 10 hall be prospective only, and hall not affect, to use detriment of any director, any limitation on the personal liability of a director of the Corporation existing at the time of such repeal, modification or adoption.

Dated: May 23, 2001

By: _____
Gregory L. Williams
Chief Executive Officer

CONTRIBUTION AGREEMENT

This Contribution Agreement (the "Agreement") is effective as of December 31, 2001 (the "Effective Date") at 11:59 PM United States of America EST (the "Effective Time") by and between Intersil Communications, Inc., a Delaware corporation ("Intersil"), and Intersil Americas Inc., a Delaware corporation ("Intersil Americas").

Background

To promote greater efficiency and economy in the management of the businesses carried on by the parties to this Agreement, Intersil desires to make a capital contribution to Intersil Americas of certain intellectual property and other assets used in the business of Intersil and its affiliates.

Terms

Intending to be legally bound, the parties to this Agreement agree as follows:

1. Effective as of the date first written above, Intersil shall contribute the following to Intersil Americas, in deemed exchange for stock of Intersil Americas in a non-recognition transaction as described in Section 351 of the Internal Revenue Code of 1986, as amended:

(i) all right, title and interest in and to the trademarks shown in Schedule A and all slogans, logotypes, designs, and trade dress associated therewith (the "Trademarks"), together with the U.S. federal registrations and applications for registration of the Trademarks, in and to all income, royalties, damages and payments now or hereafter due or payable with respect thereto and in and to all rights of action arising from the Trademarks, to be held and enjoyed by Intersil Americas for its own use and benefit and for its successors and assigns as the same would have been held by Intersil had this contribution not been made, and the goodwill of the business symbolized by the Trademarks;

(ii) all right, title and interest in and to the U.S. patents and patent applications shown in Schedule A (the "Patents"), including all reissues, divisions, continuations, continuations-in-part, and extensions thereof, to be held and enjoyed by Intersil Americas as fully and entirely as they would have been held and enjoyed by Intersil if this contribution had not been made, including all licenses of and proceeds from the Patents, all claims, demands and rights to recovery that Intersil has or may have in profits and damages for past and future infringements, if any, and all rights to compromise, sue for, and collect such profits and damages;

(iii) all right, title, and interest in and to all inventions shown in Schedule A (the "Inventions"), and all intellectual property rights relating thereto, including, without limitation, trade secret rights in the Inventions, and all rights of action arising from the Inventions, to be held and enjoyed by Intersil Americas for its own use and benefit and for its successors and assigns as the same would have been held by Intersil had this contribution not been made; and

(iv) all right, title, and interest in and to all copyrights owned by Intersil as of the date first written above that are not otherwise excluded from contribution under the terms of this Agreement, whether or not such copyrights have been registered (collectively, the "Copyrights"),

including, without limitation, all U.S. registrations and applications for registration of the Copyrights, all licenses of and proceeds from the Copyrights, all publishing, electronic publishing, and other proprietary rights arising from or related to the Copyrights, all causes of action relating to the Copyrights that may have arisen prior to this contribution, and any recovery resulting from such causes of action.

Notwithstanding the foregoing or any specific item listed on Schedule A, the intellectual property used in connection with providing products or services that are regulated by the United States Department of State shall not be contributed to Intersil Americas.

2. Intersil and Intersil Americas shall each take any and all additional actions as may be necessary or appropriate to effect the transactions contemplated by this Agreement. Such actions may include, without limitation, the execution of additional documents to record the contribution made in this Agreement and the filing of such documents with the appropriate governmental authorities.

[Signatures commence on the following page]

IN WITNESS WHEREOF, the parties have caused this Agreement to be executed as of the date below to be effective as of the Effective Date and Effective Time.

INTERSIL COMMUNICATIONS, INC.
a Delaware corporation

By: _____ Date: 12/21/01
Name: PAUL A. BERNKOPF
Title: ASST. SECRETARY

INTERSIL AMERICAS INC.
a Delaware Corporation

By: _____ Date: 12/21/01
Name: PAUL A. BERNKOPF
Title: ASST. SECRETARY

SCHEDULE A
TRADEMARKS

CaseNumber	TrademarkStatus	TrademarkName	AppNumber	RegNumber
T458	Pending	PRISM	76/049825	
T457	Pending	UNLEASHING THE POWER OF CONNECTIVITY	76/020163	
T470	Pending	ENDURA (AND DESIGN)	76/131333	
T473	Pending	DOES YOUR HOME NETWORK DO THIS	76/168307	
T476	Pending	COMMLINK (And Design)	76/177125	
T477	Pending	AIRLOCK	75/813888	
T452	Pending	STAR*POWER AND DESIGN	75/886802	
T440	Pending	WHEN FAILURE IS NOT AN OPTION	75/792441	
T441-2	Pending	INTERSIL	75/721773	
T441-3	Pending	INTERSIL	75/721751	
T442	Pending	INTERSIL (AND DESIGN)	75/746727	
T442-2	Pending	INTERSIL (AND DESIGN)	75/746761	
T442-3	Pending	INTERSIL (AND DESIGN)	75/746792	
T445	Pending	I (AND DESIGN)	75/773846	
T445-2	Pending	I (AND DESIGN)	75/773844	
T445-3	Pending	I (AND DESIGN)	75/773843	
T446	Pending	STAR*POWER	75/851663	
T447	Pending	WIRELESS AT THE SPEED OF LIFE	75/873518	
T448	Pending	DENSETRENCH	75/853697	
T459	Pending	INTERBOND	76/068207	
T451	Pending	STAR*LITE AND DESIGN	75/900860	
T472	Pending	INTELLITRIP	76/132081	
T475	Pending	PRISM/WORK	76/160295	
T450	Pending	STAR*LITE	75/900859	
T474	Pending	PRISM/HOME	76/160296	
T441-2 US	Pending	INTERSIL	75/746761	
T471	Pending	THE POWER TO PROTECT	76/132080	
T483	Pending	PRISM AND DESIGN	76/180032	
T469	Pending	ENDURA	76/122189	
T468	Pending	COMMLINK	76/135647	
T465	Pending	INTERFACE AND DESIGN	76/099311	
T464	Pending	INTERFACE	76/099352	

SCHEDULE A
TRADEMARKS

CaseNumber	TrademarkStatus	TrademarkName	AppNumber	RegNumber
T441-3 US	Pending	INTERSIL	75/746792	
T248	REGISTERED	INTERSIL	16741	1014040
T387	Registered	PRISM	75/230863	2197112
T359	Registered	PRISM (AND DESIGN)	75/088186	2108394
T325	Registered	SYNCHROFET	74/612382	2011392
T441	Registered	INTERSIL	75/722352	2488585

SCHEDULE A
PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	AppNo	FiDate	PatNo	IsDate	Title
XRCA77096		Granted	545048	24-Oct-1983	4472459	18-Sep-1984	LOCAL OXIDATION OF SILICON SUBSTRATE USING LPCVD S
XRCA74917		Granted	324059	23-Nov-1981	4429284	31-Jan-1984	OPERATIONAL AMPLIFIER
SE-102	A	Granted	973822	27-Dec-1978	4881111	14-Nov-1989	RADIATION HARD, HIGH EMITTER-BASE BREAKDOWN BIOPOLAR TRANSISTOR
SE145	A	Granted	200386	24-Oct-1980	4670769	02-Jun-1987	FABRICATION OF ISOLATED REGIONS FOR USE IN SELF-ALIGNING DEVICE PROCESS UTILIZING SELECTIVE OXIDATION
SE-198		Granted	382603	27-May-1982	4528504	09-Jul-1985	PULSED LINEAR INTEGRATED CIRCUIT TESTER
SE-198	A	Granted	744336	13-Jun-1985	4616178	07-Oct-1986	PULSED LINEAR INTEGRATED CIRCUIT TESTER
SE200		Granted	353604	01-Mar-1982	4461000	17-Jul-1984	ROM/PLA STRUCTURE AND METHOD OF TESTING
SE-201		Granted	363815	31-Mar-1982	4514802	30-Apr-1985	INTEGRATED PROGRAM COUNTER MEMORY MGMT REGISTER AND INCREMENTER
SE202		Granted	416034	08-Sep-1982	4567578	28-Jan-1986	CACHE MEMORY FLUSH SCHEME
SE-208		Granted	296192	25-Aug-1981	4472648	18-Sep-1984	TRANSISTOR CIRCUIT FOR REDUCING GATE LEAKAGE CURRENT IN A JFET
SE212		Granted	326345	01-Dec-1981	4464631	07-Aug-1984	CIRCUIT FOR TRIMMING JFET DIFFERENTIAL PAIR OFFSET VOLTAGE WITHOUT INCREASING THE OFFSET VOLTAGE TEMPERATURE COEFFICIENT
SE213		Granted	301761	14-Sep-1981	4682057	21-Jul-1987	CIR DESIGN TECH TO PREVENT CURRENT HOGGING WHEN MINIMIZE INTERCON STRIPES BY PARALL STL OR ISL GATE INPUTS
SE215		Granted	396072	07-Jul-1982	4524246	18-Jun-1985	SLIC II - COMMON MODE CURRENT REJECTION DURING RINGING

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	FilDate	Patent	IssDate	Title
SE216		Granted	309194	06-Oct-1981	4456918	26-Jun-1984	ISOLATED GATE JFET STRUCTURE
SE216	A	Granted	599817	13-Apr-1984	4495694	29-Jan-1985	ISOLATED GATE JFET STRUCTURE
SE-219		Granted	406333	09-Aug-1982	4532003	30-Jul-1985	METHOD OF FAB BIPOLAR TRANSISTOR W/IMPROVED BASE COLLECTOR BRKDN VOLTAGE AND COLLECTOR SERIES RESISTANCE
SE-221	A	Granted	782192	30-Sep-1985	4652895	24-Mar-1987	DEEP N+ BURIED ZENER STRUCTURE
SE-222	B	Granted	827285	07-Feb-1986	4862231	29-Aug-1989	METHOD OF FAB AN IC INCL ELEC-OPTIC TRANSMITTERS AND RECEIVERS
SE-222	C	Granted	07/143328	13-Jan-1988	4845052	04-Jul-1989	METHOD OF FAB AN IC INCL ELEC-OPTIC TRANSMITTERS AND RECEIVERS
SE-224		Granted	414862	03-Sep-1982	4528461	09-Jul-1985	INTEGRATED CIRCUIT SWITCH USING STACKED SCRS
SE-224	A	Granted	460020	21-Jan-1983	4528462	09-Jul-1985	INTEGRATED CIRCUIT SWITCH USING STACKED SCRS
SE225		Granted	500910	03-Jun-1983	4580131	01-Apr-1986	A BINARILY-WEIGHTED D TO A CONVERTER LADDER WITH INHERENTLY REDUCED SWITCHING NOISE
SE229	A	Granted	883279	07-Jul-1986	4729008	01-Mar-1988	HIGH VOLTAGE INTEGRATED CIRCUIT JFET STRUCTURES AND A CIRCUIT USING HIGH VOLTAGE JFETS TO ACHIEVE TRANSISTOR OPERATION T
SE229	B	Granted	130521	09-Dec-1987	4808547	28-Feb-1989	HIGH VOLTAGE INTEGRATED CIRCUIT JFET STRUCTURES AND A CIRCUIT USING HIGH VOLTAGE JFETS TO ACHIEVE TRANSISTOR OPERATION T
SE231		Granted	351442	23-Feb-1982	4471236	11-Sep-1984	HIGH TEMPERATURE BIAS LINE STABILIZED CURRENT SOURCES
SE232		Granted	351443	23-Feb-1982	4450414	22-May-1984	HIGH TEMPERATURE CURRENT MIRROR AMPLIFIER
SE227		Granted	447947	08-Dec-1982	4586193	29-Apr-1986	FORMANT-BASED SPEECH SYNTHESIZER

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Client Ref	Suffix	St Status	Ap	Fi Date	Pat	Issue	Title
SE228		Granted	526065	24-Aug-1983	4703505	27-Oct-1987	SPEECH DATA ENCODING SCHEME
SE233		Granted	460061	21-Jan-1983	4559608	17-Dec-1985	ARITHMETIC LOGIC UNIT
SE234		Granted	475618	15-Mar-1983	4581548	08-Apr-1986	ADDRESS DECODER
SE236		Granted	506794	22-Jun-1983	4567385	28-Jan-1986	POWER SWITCHED LOGIC GATES
SE-237		Granted	566400	28-Dec-1983	4596068	24-Jun-1986	PROCESS FOR MINIMI BORON DEPLETION IN N-CHANNEL FET AT SILICON OXIDE INTERFACE
SE-241		Granted	435221	19-Oct-1982	4466179	21-Aug-1984	METHOD FOR PROVID POLYSILICON THIN FILMS OF IMPROVED UNIFORMITY VE UNIFORMITY OF LASER-ANNEALED POLYSILICON THIN FILM
SE-241	A	Granted	612877	22-May-1984	4536231	20-Aug-1985	METHOD FOR PROVID POLYSILICON THIN FILMS OF IMPROVED UNIFORMITY VE UNIFORMITY OF LASER-ANNEALED POLYSILICON THIN FILM
SE-243		Granted	447946	08-Dec-1982	4546539	15-Oct-1985	12L STRUCTURE AND FABRICATION PROC COMPAT W/HI VOLT BIPOLAR TRANS
SE-245		Granted	467295	17-Feb-1983	4464825	14-Aug-1984	PROCESS FOR FAB OF HI-SPEED RADIATION HARD BIPOLAR SEMI DEVICES
SE-249	A	Granted	771160	30-Aug-1985	4620179	28-Oct-1986	METHOD FOR ANALOG TO DIGITAL CONVERSION
SE254/256		Granted	518598	29-Jul-1983	4590664	27-May-1986	METHOD OF FAB LOW NOISE REFERENCE DIODES AND TRANSISTORS
SE-251		Granted	493234	10-May-1983	4495537	22-Jan-1985	CONTROLLED CURRENT LIMITER IPATION
SE-247		Granted	454533	30-Dec-1982	4503387	05-Mar-1985	AC TESTING OF LOGIC ARRAYS
SE258		Granted	518725	29-Jul-1983	4468414	28-Aug-1984	DIELECTRIC ISOLATION FAB FOR LASER TRIMMING Y

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Apl.	Fl Date	Pat.	Iss Date	Title
SE257		Granted	506793	22-Jun-1983	4584660	22-Apr-1986	REDUCTION OF SERIES PROPAGATION DELAY AND IMPEDANCE
SE-252		Granted	504312	02-Aug-1983	4532481	30-Jul-1985	HIGH VOLTAGE CURRENT MIRROR
SE-253		Granted	526066	24-Aug-1983	4566796	28-Jan-1986	METHOD OF DETERMINING POSITION OF A WAFER BY INTERROGATING A TARGET
SE264/265	A	Granted	678075	04-Dec-1984	4554059	19-Nov-1985	ELECTROCHEM DI SINGLE TYPE ISOLATED ISLANDS
SE269		Granted	728271	29-Apr-1985	4717847	05-Jan-1988	TTL COMPATIBLE CMOS INPUT BUFFER
SE271		Granted	610583	15-May-1984	4594265	10-Jun-1986	LASER TRIMMING RESISTORS OVER DIELECTRICALLY ISOLATED ISLAND S
SE273		Granted	668864	06-Nov-1984	4639684	27-Jan-1987	AN IMPROVED DIFFERENTIAL INPUT STAGE FOR THE REALIZATION OF LOW NOISE AND HIGH PRECISION BIPOLAR TRANSISTOR AMPLIFIERS
SE275		Granted	593516	26-Mar-1984	4631636	23-Dec-1986	HIGH DENSITY PACKAGING TECHNIQUE FOR ELECTRONICS SYSTEM
SE-277		Granted	694096	23-Jan-1985	4632557	30-Dec-1986	ALIGNMENT TARGET IMAGE ENHANCEMENT FOR MICROLITHOGROPHY PROCESS
SE278		Granted	676846	01-Feb-1985	4639896	27-Jan-1987	REDUND ROW DECODING FOR PROGRAMMABLE DEVICES
SE280		Granted	788585	17-Oct-1985	4734885	29-Mar-1988	PROGRAMMING ARRANGEMENT FOR PROGRAMMABLE DEVICES
SE281	A	Granted	914524	03-Oct-1986	4757363	12-Jul-1988	DIFFUSED RESISTOR AND NPN TRANSISTOR ESD PROTECTION NETWORK FOR MOS CIRCUITS WITH SCR PREVENTION GUARD RINGS
SE282		Granted	598985	11-Apr-1984	4613772	23-Sep-1986	CURRENT COMPENSATION FOR LOGIC GATES
SE286		Granted	620728	14-Jun-1984	4591826	27-May-1986	GRAY CODE DAC LADDER

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Ap...	Fi Date	Pat...	IssDate	Title
SE289	A	Granted	07/302386	27-Feb-1989	4941027	10-Jul-1990	HIGH VOLTAGE MOS STRUCTURE
SE288		Granted	675222	27-Nov-1984	4618743	21-Oct-1986	MONOLITHIC TRANSIENT PROTECTOR
SE-298		Granted	625222	27-Jun-1984	4665327	12-May-1987	CURRENT TO VOLTAGE INTERFACE
SE299		Granted	903785	05-Sep-1986	4757528	12-Jul-1988	THERMALLY COUPLED INFORMATION TRANSMISSION ACROSS ELECTRICAL ISOLATION BOUNDARIES
SE292		Granted	720679	08-Apr-1985	4644383	17-Feb-1987	SUBCOLLECTOR FOR OXIDE AND JUNCTION ISOLATED IC'S
SE-291		Granted	620835	15-Jun-1984	4599789	15-Jul-1986	PROCESS OF MAKING TWIN WELL VLSI CMOS
SE300		Granted	630280	12-Jun-1984	4560948	24-Dec-1985	CIRCUIT FOR INCREASING VOLTAGE GAIN
SE-301/302		Granted	669787	09-Nov-1984	4595608	17-Jun-1986	METHOD FOR SEL DEPOS OF TUNGSTEN ON SILICON DEVICES
SE210B		Granted	431229	30-Sep-1982	4401940	30-Aug-1983	VOLTAGE EQUALIZER BRIDGE
SE308		Granted	673386	20-Nov-1984	4633107	30-Dec-1986	A CMOS POWER-UP RESET CIRCUIT FOR GATE ARRAYS AND STANDARD CELLS
SE310		Granted	777685	19-Sep-1985	4644191	17-Feb-1987	PROGRAM ARRAY LOGIC W/SHARED PRODUCT TERMS
SE311		Granted	777686	19-Sep-1985	4644192	17-Feb-1987	PROGRAMMABLE ARRAY LOGIC W/SHARED PROD TERMS J-K REG OUTPUTS
SE314/315		Granted	771846	09-Sep-1985	4684055	04-Aug-1987	METHOD OF A SEL SOLDER UNDERSIDE OF SUBSTRATE HAVING LEADS
SE-317		Granted	828186	11-Feb-1986	4666737	19-May-1987	VIA METALIZATION USING METAL FILLETS

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	FilDate	Pat	IssDate	Title
SE307		Granted	739843	31-May-1985	4719598	12-Jan-1988	BIT ADDRESSABLE PROGRAMMING ARRANGEMENT
SE-320		Granted	669788	09-Nov-1984	4608530	26-Aug-1986	PROGRAMMABLE CURRENT MIRROR
SE-321		Granted	824870	31-Jan-1986	4760433	26-Jul-1988	ESD PROTECTION TRANSISTORS
SE-323	C	Granted	07/919001	23-Jul-1992	5448100	05-Sep-1995	BREAKDOWN DIODE STRUCTURE
SE324		Granted	787927	16-Oct-1985	4665425	12-May-1987	FAB VERTICAL NPN/PNP BIPOLAR TRANS IN MONOLITHIC SUBSTRATE TH FT IN THE 1-GHZ RANGE
SE324	A	Granted	000377	05-Jan-1987	4717680	05-Jan-1988	FAB VERTICAL NPN/PNP BIPOLAR TRANS IN MONOLITHIC SUBSTRATE TH FT IN THE 1-GHZ RANGE
SE-329		Granted	702601	19-Feb-1985	4694313	15-Sep-1987	CONDUCTIVITY MODULATED SEMICONDUCTOR STRUCTURE
SE-330	A	Granted	048482	05-May-1987	4713681	15-Dec-1987	STRUCTURE FOR HIGH BREAKDOWN PN DIODE WITH RELATIVELY HIGH SURFACE DOPING
SE332	A	Granted	944399	19-Dec-1986	4754388	28-Jun-1988	REG CIRCUIT FOR CONVERT ALTERNATE INPUT TO A CONSTANT DIRECT OUTPUT
SE-336		Granted	798668	15-Nov-1985	4703566	03-Nov-1987	COVEYOR FOR VAPOR PHASE REFLOW SYSTEM OR NON-METALLIC LEAD COATINGS ON SEMICONDUCTOR PACKAG
SE-344		Granted	643362	22-Aug-1984	4578859	01-Apr-1986	IMPLANT MASK REVERSAL
SE341		Granted	723581	12-Apr-1985	4606936	19-Aug-1986	STRESS FREE DIELECTRIC ISOLATION TECHNOLOGY
SE346		Granted	777269	18-Sep-1985	4807012	21-Feb-1989	IC WHICH ELIMINATES SUPPORT BIAS INFLUENCE ON DIELECTRICALLY ISOLATED COMPONENTS
SE346	A	Granted	07/311812	17-Feb-1989	4923820	08-May-1990	IC WHICH ELIMINATES SUPPORT BIAS INFLUENCE ON DIELECTRICALLY ISOLATED COMPONENTS

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	F Date	Pat	Iss Date	Title
SE-358		Granted	774474	10-Sep-1985	4677321	30-Jun-1987	A TTL COMPATIBLE INPUT BUFFER
SE352		Granted	793316	31-Oct-1985	4682059	21-Jul-1987	A COMPARATOR INPUT STAGEFOR INTERFACE WITH SIGNAL CURRENT
SE-359		Granted	782691	01-Oct-1985	4650696	17-Mar-1987	PROCESS USING TUNGSTEN FOR MULTILEVEL METALIZATION
SE-363		Granted	936609	01-Dec-1986	4781853	01-Nov-1988	METHOD OF ETCH & ENHANC SILICON ETCHING CAP OF ALKALI HYDROXIDE THROUGH ADD OF POSITIVE VALENCE IMPURITY IONS
SE-363	A	Granted	187268	28-Apr-1988	4859280	22-Aug-1989	METHOD OF ETCH & ENHANC SILICON ETCHING CAP OF ALKALI HYDROXIDE THROUGH ADD OF POSITIVE VALENCE IMPURITY IONS
SE-370		Granted	723238	15-Apr-1985	4705596	10-Nov-1987	SIMULTANEOUS PLASMA SCULPTURING AND DUAL TAPERED VIA ETCH
SE377		Granted	782689	01-Oct-1985	4636744	13-Jan-1987	FRONT END OF AN OPERATIONAL AMPLIFIER
SE704		Granted	771712	03-Sep-1985	4624749	25-Nov-1986	ELECTRODEPOSITION OF SUBMICROMETER METALLIC INTERCONNECT FOR INTEGRATED CIRCUITS
SE-705		Granted	768326	22-Aug-1985	4716071	29-Dec-1987	METHOD FOR ENSURING ADHESION OF CHEMICALLY VAPOR DEPOSITED OXIDE TO GOLD INTEGRATED CIRCUIT INTERCONNECT LINES
SE-705	A	Granted	045526	04-May-1987	4713260	15-Dec-1987	METHOD FOR ENSURING ADHESION OF CHEMICALLY VAPOR DEPOSITED OXIDE TO GOLD INTEGRATED CIRCUIT INTERCONNECT LINES
SE-385		Granted	896097	13-Aug-1986	4755770	05-Jul-1988	LOW NOISE CURRENT SPECTRAL DENSITY INPUT BIAS CURRENT CANCEL SCHEME
SE-394		Granted	723239	15-Apr-1985	4705597	10-Nov-1987	PHOTORESIST TAPERING PROCESS
SE-395		Granted	831384	07-Jan-1986	4823173	18-Apr-1989	HIGH VOLTAGE LATERAL MOS STRUCTURE WITH DEPLETED TOP GATE REGION
SE-395	B	Granted	07/705509	24-May-1991	5264719	23-Nov-1993	HIGH VOLTAGE LATERAL MOS STRUCTURE WITH DEPLETED TOP GATE REGION

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Apl	FiDate	Pat#	IssDate	Title
SE396		Granted	842272	21-Mar-1986	4733168	22-Mar-1988	TEST ENABLING CIRCUIT FOR ENABLING OVERHEAD TEST CIRCUITRY IN PROGRAMMABLE DEVICES
SE397		Granted	842267	21-Mar-1986	4698589	06-Oct-1987	TEST CIRCUITRY FOR TESTING FUSE LINK PROGRAM MEMORY DEVICES
SE399		Granted	07/347574	05-May-1989	5028824	02-Jul-1991	PROGRAMMABLE DELAY CIRCUIT
SE-383		Granted	798242	08-Nov-1985	4720739	19-Jan-1988	DENSE REDUCED LEAKAGE CMOS STRUCTURE
SE-384	A	Granted	110775	21-Oct-1987	4873564	10-Oct-1989	CONDUCTIVITY-MODULATED FET WITH IMPROVED PINCH OFF-ON PERFORMANCE
SE405		Granted	763861	09-Aug-1985	4686384	11-Aug-1987	FUSE PROGRAMMABLE DC LEVEL GENERATOR
SE406		Granted	790115	22-Oct-1985	4734886	29-Mar-1988	AUX WORDLINE DRIVER FOR EFFECTIVE CONTROL PROGRAM FUSE LINKS
SE407		Granted	754711	15-Jul-1985	4675798	23-Jun-1987	DIRECT COUPLED SWITCH PWR SUPPLY W/GTO SCR SWITCH ELEMENT
SE412		Granted	782690	01-Oct-1985	4636743	13-Jan-1987	FRONT END STAGE OF AN OPERATIONAL AMPLIFIER
SE412	A	Granted	917441	07-Oct-1986	4783637	08-Nov-1988	FRONT END STAGE OF AN OPERATIONAL AMPLIFIER
SE-413		Granted	813718	27-Dec-1985	4683485	28-Jul-1987	TECH FOR INCREASING GATE-DRAIN BKDN VOLTAGE OF ION-IMPLANT JFET
SE-709	A	Granted	019697	27-Feb-1987	4814285	21-Mar-1989	METHOD FOR FORMING PLANARIZED INTERCONNECT LEVEL USING SELECTIVE DEPOSITION AND ION IMPLANTATION
SE-710	C	Granted	07/928992	12-Aug-1992	5247199	21-Sep-1993	PROCESS FOR FORMING TWIN WELL CMOS INTEGRATED CIRCUITS
SE-710	D	Granted	08/080744	22-Jun-1993	5429958	04-Jul-1995	PROCESS FOR FORMING TWIN WELL CMOS INTEGRATED CIRCUITS

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	F.Date	Pat	IssDate	Title
SE415		Granted	013851	12-Feb-1987	4761570	02-Aug-1988	PROGRAM LOGIC DEVICE WITH PROG SIGNAL INHIB AND INVERSION MEANS
SE416		Granted	051386	19-May-1987	4823300	18-Apr-1989	PERFORMING BINARY MULTI-PLICATION USING MINIMAL PATH ALGORITHM
SE713		Granted	792988	30-Oct-1985	4669884	02-Jun-1987	VARIABLE WAVELENGTH OPTICAL ALIGN SYSTEM
SE418		Granted	901841	28-Aug-1986	4728820	01-Mar-1988	LOGIC STATE TRANS DETECTION CIRCUIT FOR CMOS DEVICES
SE421		Granted	046691	07-May-1987	4780688	25-Oct-1988	LARGE SIGNAL OUTPUT CURRENT ENHANCEMENT FOR A DIFFERENTIAL PAIR
SE425		Granted	786701	09-Oct-1985	4658253	14-Apr-1987	INTERNAL SYNCH MATRIX STRUCT USED IN EXTER ASYNC PROG DEVICES
SE714		Granted	874393	16-Jun-1986	4702967	27-Oct-1987	MULTILAYER MULTIPHASE TITANIUM/NITROGEN ADHESION/DIFFUSIONS TRUCTUN A GOLD-BASED MICROCIRCUIT INTERCONNECT METALLIZATION
SE-716	A	Granted	181718	14-Apr-1988	4970573	13-Nov-1990	SELF-PLANARIZED ELECTROPLATED GOLD INTERCONNECT LAYER
SE-717	A	Granted	224320	26-Jul-1988	4818725	04-Apr-1989	A PLANAR GATE STRUCTURE
SE718		Granted	841297	19-Mar-1986	4702000	27-Oct-1987	TECHNIQUE FOR ELIMINATION OF POLYSILICON STRINGERS IN DIRECT MOAT FIELD OXIDE STRUCTURE
SE718	A	Granted	084556	11-Aug-1987	4908683	13-Mar-1990	TECHNIQUE FOR ELIMINATION OF POLYSILICON STRINGERS IN DIRECT MOAT FIELD OXIDE STRUCTURE
SE441		Granted	896103	13-Aug-1986	4701644	20-Oct-1987	LOW POWER SENSE AMPLIFIER
SE451		Granted	027940	19-Mar-1987	4804865	14-Feb-1989	FAST VOLTAGE REFERENCE STABILIZATION TECHNIQUE
SE455		Granted	07/437472	15-Nov-1989	5051949	24-Sep-1991	CONTENT ADDRESSABLE MEMORY DEVICE

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	FilDate	Patent	IssDate	Title
SE-456		Granted	118251	09-Nov-1987	4855625	08-Aug-1989	OPERATIONAL AMPLIFIER HAVING LOW DC CURRENT INPUT CIRCUIT
SE-438		Granted	000778	06-Jan-1987	4789426	06-Dec-1988	PROCESS FOR PERFORM VARIABLE SELEC POLYSILICON ETCH
SE-457	A	Granted	07/819748	13-Jan-1992	5214329	25-May-1993	BIAS CURRENT MODULATION FOR DIFFERENTIALLY COUPLED TRANSISTOR CIRCUIT
SE-466		Granted	919465	16-Oct-1986	4708747	24-Nov-1987	DIELECTRIC FOR LASER TRIMMING
SE-466	B	Granted	07/296855	13-Jan-1989	4839711	13-Jun-1989	DIELECTRIC FOR LASER TRIMMING
SE-472		Granted	042135	24-Apr-1987	4771016	13-Sep-1988	USING A RAPID THERMAL PROCESS FOR MFG WAFER BONDED SOL SEMIC ONDUCT
SE723		Granted	947749	30-Dec-1986	4786608	22-Nov-1988	TECH FOR FORMING ELEC FIELD SHIELD LAYER IN OXY-IMPLANT SILICON SUR IN OXYGEN-IMPLANTED SILICON SUBSTRATES
SE-477		Granted	523427	15-May-1990	5014108	07-May-1991	METHOD OF MAKING SILICON MESFET FOR DIELECTRICALLY ISOLATED INTEGRATED CIRCUITS
SE-477	A	Granted	07/606193	31-Oct-1990	5306650	26-Apr-1994	METHOD OF MAKING SILICON MESFET FOR DIELECTRICALLY ISOLATED INTEGRATED CIRCUITS
SE-480		Granted	151184	01-Feb-1988	4912053	27-Mar-1990	ION IMPLANTED JFET WITH SELF-ALIGNED SOURCE AND DRAIN
SE-481		Granted	07/387534	31-Jul-1989	4968900	06-Nov-1990	PROGRAMMABLE SPEED/POWER ARRANGEMENT FOR INTEGRATED DEVICES HAVING LOGIC MATRICES
SE487		Granted	07/301835	26-Jan-1989	4876579	24-Oct-1989	LOW TOP GATE RESISTANCE GATE JFET STRUCTURE
SE489/491		Granted	057398	12-May-1987	4795718	03-Jan-1989	SELF-ALIGNED CONTACT FOR MOS PROCESSING
SE-490		Granted	062309	15-Jun-1987	4752591	21-Jun-1988	SELF-ALIGNED CONTACTS FOR BIPOLAR PROCESS

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	MxStatus	Appl	Fildate	Patno	Issdate	Title
SE-725		Granted	055356	29-May-1987	4753851	28-Jun-1988	MULTI LAYER TUNGSTEN/TITANIUM TITANIUM/NITRIDE ADHESION/DIFFUSION BARRI LAYER STRUCT FOR GOLD-BASE MICROCIRCUIT
SE-500		Granted	O7/403865	07-Sep-1989	5051619	24-Sep-1991	PREDRIVE CIRCUIT HAVING LEVEL SENSING CONTROL
SE-500	A	Granted	90/002598	10-Feb-1992	B1 5051619	02-Mar-1993	PREDRIVE CIRCUIT HAVING LEVEL SENSING CONTROL
SE-505	A	Granted	07/334148	06-Apr-1989	4914501	03-Apr-1990	VERTICAL CONTACT STRUCTURE
SE-508		Granted	025539	13-Mar-1987	4851257	25-Jul-1989	PROCESS FOR THE FABRICATION OF A VERTICAL CONTACT
SE-511		Granted	025435	13-Mar-1987	5066995	19-Nov-1991	DOUBLE LEVEL CONDUCTOR STRUCTURE
SE-516		Granted	075641	20-Jul-1987	4818901	04-Apr-1989	CONTROLLED SWITCHING CMOS OUTPUT BUFFER
SE-727		Granted	036508	09-Apr-1987	4812962	14-Mar-1989	AREA FEATURE SORTING MECHANISM FOR NEIGHBORHOOD-BASED PROXIMITY CORRECTION IN LITHOGRAPHY PROCESING OF INTEGRATED CIRCUIT PATTERNS
SE-525		Granted	257015	13-Oct-1988	4897567	30-Jan-1990	FAST LEVEL TRANSLATOR CIRCUIT
SE-526		Granted	049637	13-May-1987	4854986	08-Aug-1989	BONDING TECHNIQUE TO JOIN TWO OR MORE SILICON WAFERS
SE-529		Granted	067838	29-Jun-1987	4851078	25-Jul-1989	DIELECTRIC ISOLATION PROCESS USING DOUBLE WAFER BONDING
SE-533		Granted	213823	03-Jun-1988	4857764	15-Aug-1989	CURRENT COMPENSATED PRECHARGED BUS
SE-541		Granted	092975	03-Sep-1987	4897362	30-Jan-1990	DOUBLE EPITAXIAL METHOD OF FAB SEMICONDUCTOR DEVICES ON BONDED WAFERS
SE-543		Granted	106071	07-Oct-1987	4882698	21-Nov-1989	CELL BASED ALU WITH TREE STRUCTURED CARRY, INVERT LOGIC AND BALANCED LOADING

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Client Ref	Sub Case	Status	Appl	Filing Date	Patent	Issue Date	Title
SE-544		Granted	124807	24-Nov-1987	5047974	10-Sep-1991	CELL BASED ADDER W/TREE STRUCTURED CARRY INVERTING LOGIC AND BALANCED LOADING
SE-547		Granted	164342	04-Mar-1988	4948746	14-Aug-1990	ISOLATED GATE MESFET AND METHOD OF MAKING AND TRIMMING
SE-547	A	Granted	07/537936	14-Jun-1990	5010377	23-Apr-1991	ISOLATED GATE MESFET AND METHOD OF MAKING AND TRIMMING
SE-553		Granted	132186	14-Dec-1987	4868778	19-Sep-1989	SPEED ENHANCEMENT FOR MULTIPLIERS USING MINIMAL PATH ALGORITHM
SE-555		Granted	07/382388	20-Jul-1989	5081063	14-Jan-1992	METHOD OF MAKING EDGE-CONNECTED INTEGRATED CIRCUIT STRUCTURE
SE-555	B	Granted	07/802882	06-Dec-1991	5185292	09-Feb-1993	METHOD OF MAKING EDGE-CONNECTED INTEGRATED CIRCUIT STRUCTURE
SE-557	B	Granted	07/834439	12-Feb-1992	5266135	30-Nov-1993	WAFER BONDING USING TRAPPED OXIDIZING VAPOR
SE-557	C	Granted	08/137293	14-Oct-1993	5334273	02-Aug-1994	WAFER BONDING USING TRAPPED OXIDIZING VAPOR
SE-560		Granted	07/376019	06-Jul-1989	4929566	29-May-1990	METHOD OF MAKING DIELECTRICALLY ISOLATED INTEGRAT CIRCUITS USING OXYGEN IMPLAN AND EXPITAXIAL GROWTH
SE-562		Granted	103620	30-Sep-1987	4801065	31-Jan-1989	CHIP CARRIER SOLDERING PALLET SOLDER LEVELING PIN
SE-565		Granted	195265	18-May-1988	4949296	14-Aug-1990	METHOD AND APPARTUS FOR COMPUTING SQUARE ROOTS OF BINARY NUMBERS
SE-567		Granted	07/467590	19-Jan-1990	5070388	03-Dec-1991	TRENCH-RESIDENT INTERCONNECT STRUCTURE
SE-568		Granted	263189	27-Oct-1988	4879520	07-Nov-1989	HIGH ACCURACY CURRENT SOURCE AND HIGH ACCURACY TRANSCONDUCTANCE STAGE
SE-572		Granted	289747	27-Dec-1988	4891604	02-Jan-1990	HIGH SPEED LOW INPUT CURRENT VOLTAGE FOLLOWER STAGE

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	FilDate	Pat	IssDate	Title
SE-573		Granted	07/281546	08-Dec-1988	4900689	13-Feb-1990	METHOD OF FABRICATION OF DIELECTRICALLY ISOLATED COMPLEMENTARY BIPOLAR DEVICES
SE-574		Granted	07/235543	24-Aug-1988	4951102	21-Aug-1990	TRENCH GATE VCMOS METHOD OF MANUFACTURE
SE-574	A	Granted	07/533435	05-Jun-1990	5032529	16-Jul-1991	TRENCH GATE VCMOS METHOD OF MANUFACTURE
SE-580	A	Granted	07/651460	06-Feb-1991	5120669	09-Jun-1992	METHOD OF FORMING SELF-ALIGNED TOP GATE CHANNEL BARRIER REGION IN ION-IMPLANTED JFET
SE-582		Granted	07/370280	23-Jun-1989	4980651	25-Dec-1990	HIGH SPEED, HIGH PRECISION OPERATIONAL AMPLIFIER
SE-583		Granted	07/505899	06-Apr-1990	5148475	15-Sep-1992	REDUCED CONTACT RESISTANCE ON A SLIC
SE-586		Granted	07/340705	20-Apr-1989	4982194	01-Jan-1991	BACK-SAMPLING CHARGE REDISTRIBUTION ANALOG TO DIGITAL CONVERTER
SE-586	A	Granted	07/587089	24-Sep-1990	5059982	22-Oct-1991	BACK-SAMPLING CHARGE REDISTRIBUTION ANALOG TO DIGITAL CONVERTER
SE-587	A	Granted	07/416419	03-Oct-1989	5021359	04-Jun-1991	RADIATION HARDENED COMPLEMENTARY TRANSISTOR INTEGRATED CIRCUITS
SE-594/600		Granted	07/289748	27-Dec-1988	4888741	19-Dec-1989	MEMORY WITH CACHE REGISTER INTERFACE STRUCTURE
SE-603		Granted	195273	18-May-1988	4916497	10-Apr-1990	INTEGRATED CIRCUITS INCL PHOTO-OPTICAL DEVICES AND PRESSURE TRANSDUCERS AND METHOD OF FABRICATION
SE-603	A	Granted	07/465314	12-Jan-1990	5037765	06-Aug-1991	INTEGRATED CIRCUITS INCL PHOTO-OPTICAL DEVICES AND PRESSURE TRANSDUCERS AND METHOD OF FABRICATION
SE-603	C	Granted	07/606155	31-Oct-1990	5070596	10-Dec-1991	INTEGRATED CIRCUITS INCL PHOTO-OPTICAL DEVICES AND PRESSURE TRANSDUCERS AND METHOD OF FABRICATION
SE-608		Granted	282064	09-Dec-1988	4968628	06-Nov-1990	METHOD OF FABRICATING BACK DIFFUSED BONDED OXIDE SUBSTRATE

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl#	FilDate	Pat#	IssDate	Title
SE-617		Granted	271656	16-Nov-1988	4893088	09-Jan-1990	TRANSIMPEDANCE FOCAL PLANE PROCESSOR
SE-600		Granted	266812	03-Nov-1988	4937774	26-Jun-1990	EAST IMAGE PROCESSING ACCELERATOR FOR REAL TIME IMAGE PROCESSING APPLICATIONS
SE563		Granted	07/307944	09-Feb-1989	4891606	02-Jan-1990	PHOTOCURRENT COMPENSATION USING ACTIVE DEVICES
SE-570		Granted	07/272908	18-Nov-1988	4879523	07-Nov-1989	HIGH ACCURACY, HIGH IMPEDANCE DIFFERENTIAL TO SINGLE-ENDED CURRENT CONVERTER
SE-626		Granted	07/313435	22-Feb-1989	4908566	13-Mar-1990	VOLTAGE REGULATOR HAVING STAGGERED POLE-ZERO COMPENSATION NETWORK
SE-619		Granted	07/357898	26-May-1989	4929923	29-May-1990	THIN FILM RESISTORS AND METHOD OF TRIMMING
SE-620		Granted	07/336787	13-Apr-1989	4933648	12-Jun-1990	CURRENT MIRROR EMPLOYING CONTROLLED BYPASS CIRCUIT
SE-631		Granted	07/361439	05-Jun-1989	4970677	13-Nov-1990	FULL ADDER CIRCUIT WITH IMPROVED CARRY AND SUM LOGIC GATES
SE-637	A	Granted	07/973932	24-Nov-1992	5262976	16-Nov-1993	PLURAL BIT RECORDING MULTIPLIER
SE-639	A	Granted	07/972510	06-Nov-1992	5469556	21-Nov-1995	RESOURCE ACCESS SECURITY SYSTEM FOR CONTROLLING ACCESS TO RESOURCES OF A DATA PROCESSING SYSTEM
SE-642		Granted	07/436247	14-Nov-1989	5039888	13-Aug-1991	METHOD AND CIRCUIT ARRANGEMENT FOR PROVIDING PROGRAMMABLE HYSTERESIS TO A DIFFERENTIAL COMPARATOR
SE-638		Granted	07/367788	19-Jun-1989	5028973	02-Jul-1991	BIPOLAR TRANSISTOR WITH HIGH EFFICIENT EMITTER
SE-651		Granted	07/405282	11-Sep-1989	4929568	29-May-1990	METHOD OF ISOLATING A TOP GATE OF A MESFET AND THE RESULTING DEVICE
SE-651	B	Granted	07/668984	12-Mar-1991	5107312	21-Apr-1992	METHOD OF ISOLATING A TOP GATE OF A MESFET AND THE RESULTING DEVICE

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Client Ref	SubCase	Status	Appl #	Fil Date	Pat #	Iss Date	Title
SE-641		Granted	07/475007	05-Feb-1990	5084839	28-Jan-1992	VARIABLE LENGTH SHIFT REGISTER
SE-656		Granted	07/447618	08-Dec-1989	5038248	06-Aug-1991	AUTOMATIC ESD PROTECTION DEVICE FOR SEMICONDUCTORS PACKAGES
SE-659		Granted	07/451249	15-Dec-1989	4979011	18-Dec-1990	SCR STRUCTURE FOR FAST TURNON SWITCHING
SE-660		Granted	07/457504	27-Dec-1989	5060192	22-Oct-1991	CROSS-POINT SWITCH
SE-661		Granted	07/482803	21-Feb-1990	5265225	23-Nov-1993	DSP ADDRESS SEQUENCER
SE-654	A	Granted	07/679182	02-Apr-1991	5248894	28-Sep-1993	SELF-ALIGNED CHANNEL STOP FOR TRENCH-ISOLATED ISLAND
SE-654	B	Granted	08/106160	13-Aug-1993	5436189	25-Jul-1995	SELF-ALIGNED CHANNEL STOP FOR TRENCH-ISOLATED ISLAND
SE-657		Granted	07/424917	20-Oct-1989	5008719	16-Apr-1991	DUAL LAYER SURFACE GATE JFET HAVING ENHANCED GATE-CHANNEL BREAKDOWN VOLTAGE
SE-657	A	Granted	07/609801	05-Nov-1990	5118632	02-Jun-1992	DUAL LAYER SURFACE GATE JFET HAVING ENHANCED GATE-CHANNEL BREAKDOWN VOLTAGE
SE-688	A	Granted	07/336632	10-Apr-1989	5070451	03-Dec-1991	FORTH SPECIFIC LANGUAGE MICROPROCESSOR
SE-688	B	Granted	07/745764	16-Aug-1991	5319757	07-Jun-1994	FORTH SPECIFIC LANGUAGE MICROPROCESSOR
SE-625		Granted	07/431517	03-Nov-1989	5015887	14-May-1991	A-B BUFFER CIRCUIT WITH TTL COMPATIBLE OUTPUT DRIVE
SE-675/471	A	Granted	07/651327	05-Feb-1991	5306944	26-Apr-1994	SEMICONDUCTOR STRUCTURE WITHIN DI ISLANDS HAVING BOTTOM PROJECTION FOR CONTROLLING DEVICE CHARACTERISTICS
SE-663-TD	A	Granted	07/755314	05-Sep-1991	5327006	05-Jul-1994	THIN, DIELECTRICALLY ISOLATED ISLAND RESIDENT TRANSISTOR STRUCTURE HAVING LOW COLLECTOR RESISTANCE

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	Subcase	Status	ApplNo	FilDate	PatNo	IssDate	Title
SE-670	A	Granted	07/717347	18-Jun-1991	5218321	08-Jun-1993	LOW OFFSET UNITY GAIN BUFFER AMPLIFIER
SE-682	A	Granted	07/640041	11-Jan-1991	5198385	30-Mar-1993	PHOTOLITHOGRAPHIC FORMATION OF DIE-TO-PACKAGE AIRBRIDGE
SE-664		Granted	07/561821	02-Aug-1990	5113361	12-May-1992	SIN/COS GENERATOR IMPLEMENTATION
SE-665		Granted	07/490316	08-Mar-1990	5034343	23-Jul-1991	MANUFACTURING ULTRA-THIN WAFE USING A HANDLE WAFER
SE-655		Granted	07/563276	06-Aug-1990	5057895	15-Oct-1991	TRENCH CONDUCTOR AND CROSSUNDER ARCHITECTURE
SE-655	A	Granted	07/738532	31-Jul-1991	5196373	23-Mar-1993	TRENCH CONDUCTOR AND CROSSUNDER ARCHITECTURE
SE-655	B	Granted	07/916198	17-Jul-1992	5283461	01-Feb-1994	TRENCH CONDUCTOR AND CROSSUNDER ARCHITECTURE
SE-695		Granted	07/498642	26-Mar-1990	5079176	07-Jan-1992	METHOD OF FORMING A HIGH VOLTAGE JUNCTION IN A DIELECTRICALLY ISOLATED ISLAND
SE-693		Granted	07/509405	16-Apr-1990	5091331	25-Feb-1992	ULTRA THIN CIRCUIT FABRICATION BY CONTROLLED WAFER DEBONDING
SE-692		Granted	07/508568	13-Apr-1990	5015877	14-May-1991	LOW DISTORTION SAMPLE AND HOLD CIRCUIT
SE-669		Granted	07/529548	29-May-1990	5081410	14-Jan-1992	BAND-GAP REFERENCE
SE-697		Granted	07/516310	30-Apr-1990	5079734	07-Jan-1992	DIGITAL DECIMATION FILTER
SE-698		Granted	07/624964	10-Dec-1990	5151953	29-Sep-1992	SINGLE CHIP 2-D CONVOLVER
SE-699		Granted	07/474172	31-Jan-1990	5248932	28-Sep-1993	CURRENT MIRROR CIRCUIT WITH CASCODED BIPOLAR TRANSISTORS.

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Client Ref	Sub Case	Status	Appl	Filing Date	Patent	Issue Date	Title
SE-700		Granted	07/474417	31-Jan-1990	5030862	09-Jul-1991	TURNOFF CIRCUIT FOR GATE TURN OFF SCR
SE-666	A	Granted	07/668694	07-Mar-1991	5081061	14-Jan-1992	MANUFACTURING ULTRA-THIN DIELECTRICALLY ISOLATED WAFERS
RD 14147		Granted	362682	29-Mar-1982	4429011	31-Jan-1984	COMPOSITE CONDUCTIVE STRUCTURES AND METHOD OF MAKING SAME
RD 14174		Granted	374586	03-May-1982	4468574	28-Aug-1984	DUAL GATE CMOS TRANSISTOR CIRCUITS HAVING REDUCED ELECTRODE CAPACITANCE
RD 14366		Granted	489613	28-Apr-1983	4471004	11-Sep-1984	METHOD OF FORMING REFRACTORY METAL CONDUCTORS OF LOW RESISTIVITY
RD 14176		Granted	374587	03-May-1982	4472821	18-Sep-1984	DYNAMIC SHIFT REGISTER UTILIZING CMOS DUAL GATE TRANSISTORS
RD 15243		Granted	653274	24-Sep-1984	4584207	22-Apr-1986	METHOD FOR NUCLEATING AND GROWING TUNGSTEN FILMS
RD 15709		Granted	615403	26-Jun-1984	4585493	29-Apr-1986	GRAIN DRIVEN ZONE MELTING OF SILICON FILMS ON INSULATING SUBSTRATES
28-ME-2005		Granted	687357	28-Dec-1984	4602210	22-Jul-1986	MULTIPLEXED ACCESS SCAN TESTABLE INTEGRATED CIRCUIT
RD 16243		Granted	790911	24-Oct-1985	4638400	20-Jan-1987	REFRACTORY METAL CAPACITOR STRUCTURES PARTICULARLY FOR ANALOG INTEGRATED CIRCUIT DEVICES
XRCA83013		Granted	830760	19-Feb-1986	4704186	03-Nov-1987	RECESSED OXIDE METHOD FOR MAKING A SILICON ON INSULATOR SUBSTRATE
28-ME-2016		Granted	935372	26-Nov-1986	4707455	17-Nov-1987	METHOD OF FABRICATING A TWIN TUB CMOS DEVICE
XRCA82113		Granted	782581	01-Oct-1985	4725875	16-Feb-1988	MEMORY CELL WITH DIODES PROVIDING RADIATION HARDNESS
RD 17522		Granted	891058	31-Jul-1986	4729005	01-Mar-1988	METHOD AND APPARATUS FOR IMPROVED METAL INSULATOR SEMICONDUCTOR DEVICE OPERATION

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl#	FileDate	Pat#	IssDate	Title
XRCA82873		Granted	856280	28-Apr-1986	4735917	05-Apr-1988	SIICON ON SAPPHIRE INTEGRATED CIRCUITS
28-ME-2014		Granted	060490	11-Jun-1987	4745089	17-May-1988	SELF ALIGNED BARRIER METAL AND OXIDATION MASK METHOD
XRCA82373		Granted	780897	27-Sep-1985	4751554	14-Jun-1988	SILICON ON SAPPHIRE INTEGRATED CIRCUIT AND METHOD OF MAKING THE SAME
RD 17954P		Granted	033378	02-Apr-1987	4751561	14-Jun-1988	DIELECTRICALLY ISOLATED PMOS, NMOS, PNP AND NPN TRANSISTORS ON A SILICON WAFER
XRCA82384		Granted	863432	15-May-1986	4755481	05-Jul-1988	METHOD OF MAKING A SILICON ON INSULATOR TRANSISTOR
XRCA83489		Granted	904156	05-Sep-1986	4760557	26-Jul-1988	RADIATION HARD MEMORY CELL CIRCUIT WITH HIGH INVERTER IMPEDANCE RATIO
XRCA83030		Granted	911423	25-Sep-1986	4775641	04-Oct-1988	METHOD OF MAKING SILICON ON SAPPHIRE SEMICONDUCTOR DEVICES
RD 17689		Granted	081076	03-Aug-1987	4782249	01-Nov-1988	STATIC CMOS PROGRAMMABLE LOGIC ARRAY
XRCA83959		Granted	108656	15-Oct-1987	4805187	14-Feb-1989	DETERMINATION OF SUBSTRATE TEMPERATURE USED DURING OXYGEN IMPLANTATION OF SIMOX WAFER
RD 18187P		Granted	137314	23-Dec-1987	4824698	25-Apr-1989	HIGH TEMPERATURE ANNEALING TO IMPROVE SIMOX CHARACTERISTICS
35ME02029		Granted	274176	21-Nov-1988	5034789	23-Jul-1991	DIELECTRIC ISOLATION FOR SOI ISLAND SIDE WALL FOR REDUCING LEAKAGE CURRENT
35ME02029	A	Granted	07/641486	15-Jan-1991	5053353	01-Oct-1991	DIELECTRIC ISOLATION FOR SOI ISLAND SIDE WALL FOR REDUCING LEAKAGE CURRENT
35ME02040		Granted	266756	03-Nov-1988	4956306	11-Sep-1990	METHOD FOR FORMING COMPLEMENTARY PATTERNS IN A SEMICONDUCTOR MATERIAL WHILE USING A SINGLE MASKING STEP
28-IS-003B		Granted	443600	09-Dec-1982	4568913	04-Feb-1986	HIGH SPEED ANALOG TO DIGITAL CONVERTER

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	Subcase	Status	Appl	Filing Date	Patent	Issue Date	Title
28-IS-005B		Granted	381386	24-May-1982	4465996	14-Aug-1984	HIGH ACCURACY DIGITAL-TO-ANALOG CONVERTER
28-IS-0011		Granted	328518	08-Dec-1981	4473757	25-Sep-1984	ACTIVE CURRENT STEERING NETWORK
28-IS-0013		Granted	328519	08-Dec-1981	4433282	21-Feb-1984	MONOLITHIC VOLTAGE DIVIDER
28-IS-0016		Granted	407332	12-Aug-1982	4595906	17-Jun-1986	SCALED ANALOG TO DIGITAL CONVERTER
28-IS-0017		Granted	434893	18-Oct-1982	4547683	15-Oct-1985	HIGH SPEED CHARGE BALANCING COMPARATOR
28-IS-0018		Granted	395670	06-Jul-1982	4535410	13-Aug-1985	POWER SUPPLY FAILURE EARLY WARNING DETECTOR
28-IS-0019		Granted	453237	27-Dec-1982	4546324	08-Oct-1985	DIGITALLY SWITCHED ANALOG SIGNAL CONDITIONER
28-IS-0023		Granted	340765	19-Jan-1982	4486670	04-Dec-1984	A MONOLITHIC CMOS LOW POWER DIGITAL LEVEL SHIFTER
28-IS-0027		Granted	578535	09-Feb-1984	4641129	03-Feb-1987	HIGH SPEED AND HIGH ACCURACY ANALOG TO DIGITAL CONVERTER
28-IS-0029		Granted	567577	03-Jan-1984	4617473	14-Oct-1986	CMOS BACKUP POWER SWITCHING CIRCUIT
28-IS-0033		Granted	615353	30-May-1984	4652808	24-Mar-1987	IMPROVED EFFICIENCY SWITCHING VOLTAGE CONVERTER
28-IS-0035		Granted	579276	13-Feb-1984	4639715	27-Jan-1987	IMPROVED FLASH ANALOG TO DIGITAL CONVERTER
28-IS-0036		Granted	669119	07-Nov-1984	4667164	19-May-1987	IMPROVED FREQUENCY RESPONSE AMPLIFIER
28-IS-0039		Granted	714866	22-Mar-1985	4787047	22-Nov-1988	ELECTRICALLY ERASABLE FUSED PROGRAMMABLE LOGIC ARRAY

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Ap#	F.I.Date	Pat#	Isspate	Title
28-IS-0040		Granted	745580	17-Jun-1985	4644353	17-Feb-1987	PROGRAMMABLE INTERFACE
28-IS-0041		Granted	719478	03-Apr-1985	4703199	27-Oct-1987	NON-RESTRICTED LEVEL SHIFTER
28-IS-0044		Granted	718171	01-Apr-1985	4646331	24-Feb-1987	ELECTRONIC STATIC SWITCHED-LATCH FREQUENCY DIVIDER CIRCUIT WITH ODD NUMBER COUNTING CAPABILITY
28-IS-0047		Granted	785381	07-Oct-1985	4656459	07-Apr-1987	DUAL SLOPE CONVERTER WITH LARGE APPARENT INTEGRATOR SWING
28-IS-0050		Granted	786175	09-Oct-1985	4633221	30-Dec-1986	DUAL SLOPE ANALOG TO DIGITAL CONVERTER WITH AUTOMATIC SHORT CYCLE RANGE DETERMINATION
28-IS-0054		Granted	892702	01-Aug-1986	4855722	08-Aug-1989	ALTERNATING CURRENT POWER LOSS DETECTOR
28-IS-0055		Granted	908489	17-Sep-1986	4831577	16-May-1989	DIGITAL MULTIPLIER ARCHITECTURE WITH TRIPLE ARRAY SUMMATION
28-IS-0060		Granted	123056	18-Nov-1987	5159204	27-Oct-1992	STRUCTURE AND METHOD FOR PREVENTING LATCH-UP IN INTEGRATED CIRCUITS
RD 15746		Granted	668454	05-Nov-1984	4552783	12-Nov-1985	ENHANCING THE SELECTIVITY OF TUNGSTEN DEPOSITION ON CONDUCT OR AND SEMICONDUCTOR SURFACES
SE-701		Granted	07/615358	19-Nov-1990	5085084	04-Feb-1992	METHOD AND APPARATUS FOR TESTING LEAD BONDS AND DETECTING FAILURE
SE-703	A	Granted	07/750752	20-Aug-1991	5138319	11-Aug-1992	TWO STAGE A/D CONVERTER UTILIZING DUAL MULTIPLEXED CONVERTERS WITH A COMMON CONVERTER
SE-735		Granted	07/891910	01-Jun-1992	5240876	31-Aug-1993	SOI WAFER WITH SIGE
SE-735	A	Granted	07/891052	01-Jun-1992	5218213	08-Jun-1993	SOI WAFER WITH SIGE
SE-742		Granted	07/598165	16-Oct-1990	5086242	04-Feb-1992	FAST TURN-OFF THYRISTOR STRUCTURE

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	FDate	Patent	IssDate	Title
SE-745/746		Granted	07/523020	14-May-1990	5119321	02-Jun-1992	ADAPTIVE THRESHOLD SUPPRESSION OF IMPULSE NOISE
SE-751		Granted	07/739133	30-Jul-1991	5241213	31-Aug-1993	BURIED ZENER DIODE HAVING AUXILIARY ZENER JUNCTION ACCESS PATH
SE-753		Granted	07/769209	01-Oct-1991	5200733	06-Apr-1993	RESISTOR STRUCTURE AND METHOD OF FABRICATION
SE-758	A	Granted	08/131369	04-Oct-1993	5668397	16-Sep-1997	HIGH FREQUENCY ANALOG TRANSISTORS, METHOD OF FABRICATION AND CIRCUIT IMPLEMENTATION
SE-758	B	Granted	08/462851	05-Jun-1995	5807780	15-Sep-1998	HIGH FREQUENCY ANALOG TRANSISTORS, METHOD OF FABRICATION AND CIRCUIT IMPLEMENTATION
SE-759		Granted	07/674147	25-Mar-1991	5311054	10-May-1994	IMPROVED GRADED COLLECTOR FOR INDUCTIVE LOADS
SE-759	A	Granted	08/191963	03-Feb-1994	5397714	14-Mar-1995	IMPROVED GRADED COLLECTOR FOR INDUCTIVE LOADS
SE-761		Granted	07/647346	29-Jan-1991	5140326	18-Aug-1992	CONVERTER COMPARATOR CELL WITH IMPROVED RESOLUTION
SE-768		Granted	07/774620	10-Oct-1991	5450339	12-Sep-1995	NONCANONIC FULLY SYSTOLIC LMS ADAPTIVE ARCHITECTURE
SE-770		Granted	07/774628	01-Jul-1991	5258939	02-Nov-1993	FOLD AND DECIMATE FILTER ARCHITECTURE
SE-766		Granted	07/604883	29-Oct-1990	5117282	26-May-1992	STACKED CONFIGURATION FOR INTEGRATED CIRCUITS DEVICES
SE-766	A	Granted	07/825133	24-Jan-1992	5228192	20-Jul-1993	STACKED CONFIGURATION FOR INTEGRATED CIRCUITS DEVICES
SE-772	A	Granted	07/816321	30-Dec-1991	5194867	16-Mar-1993	FLASH ANALOG-TO-DIGITAL CONVERTER EMPLOY LEAST SIGNIFICANT BIT REPRESENTATIVE COMPARATIVE REFERENCE VOLTAGE
SE-696		Granted	07/689645	23-Apr-1991	5233289	03-Aug-1993	VOLTAGE DIVIDER AND USE AS BIAS NETWORK FOR STACKED TRANSISTORS

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	Appl Date	Pat	Iss Date	Title
SE-696	A	Granted	08/071795	04-Jun-1993	5493207	20-Feb-1996	VOLTAGE DIVIDER AND USE AS BIAS NETWORK FOR STACKED TRANSISTORS
RD 18146		Granted	173918	28-Mar-1988	4942449	17-Jul-1990	FAB METHOD AND STRUCTURE FOR FIELD ISOLATION IN FIELD EFFECT TRANSISTORS ON IC CHIPS
SE-778		Granted	07/724206	01-Jul-1991	5206821	27-Apr-1993	DECIMATING FILTER
SE-778	A	Granted	07/945674	15-Sep-1992	5341335	23-Aug-1994	DECIMATING FILTER
SE-776		Granted	07/689624	23-Apr-1991	5096850	17-Mar-1992	METHOD OF LASER TRIMMING
SE-776	A	Granted	07/852541	17-Mar-1992	5235205	10-Aug-1993	METHOD OF LASER TRIMMING
SE-653		Granted	07/732475	18-Jul-1991	5359211	25-Oct-1994	HIGH VOLTAGE PROTECTION USING SCRS
SE-653	A	Granted	08/253287	26-Aug-1994	5670799	23-Sep-1997	HIGH VOLTAGE PROTECTION USING SCRS
SE-784	A	Granted	08/216217	21-Mar-1994	5429993	04-Jul-1995	SEMICONDUCTOR ACCELEROMETER AND METHOD OF ITS MANUFACTURE
SE-784	B	Granted	08/457643	31-May-1995	5656512	12-Aug-1997	SEMICONDUCTOR ACCELEROMETER AND METHOD OF ITS MANUFACTURE
SE-787		Granted	07/930072	14-Aug-1992	5515402	07-May-1996	QUADRATURE FILTER WITH REAL CONVERSION
28-SV-0070		Granted	07/601974	22-Oct-1990	5138413	11-Aug-1992	PISO ELECTROSTATIC DISCHARGE PROTECTION DEVICE
RD 15522		Granted	593064	26-Mar-1984	4590130	20-May-1986	SOLID STATE ZONE RECRYSTALLIZATION OF SEMICONDUCTOR MATERIA
RD 16311		Granted	890050	28-Jul-1986	4695489	22-Sep-1987	ELECTROLESS NICKEL PLATING COMPOSITION AND METHOD

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	FilDate	Patn	GrntDate	Title
RD 16392		Granted	805651	06-Dec-1985	4685040	04-Aug-1987	UNIVERSAL INTEGRATED CIRCUIT POWER SUPPLY CHIP
RD 16484		Granted	853108	17-Apr-1986	4677736	07-Jul-1987	SELF-ALIGNED INLAY TRANSISTOR WITH OR WITHOUT SOURCE AND DR
RD 16518		Granted	790716	24-Oct-1985	4661838	28-Apr-1987	HIGH VOLTAGE SEMICONDUCTOR DEVICES ELECTRICALLY ISOLATED FR
RD 16587		Granted	047739	08-May-1987	4746375	24-May-1988	ACTIVATION OF REFRACTORY METAL SURFACES FOR ELECTROLESS PLA
RD 16999		Granted	085922	17-Aug-1987	4768016	30-Aug-1988	TIMING AND CONTROL CIRCUITRY FOR FLASH ANALOG TO DIGITAL CO
RD 17119		Granted	935470	26-Nov-1986	4717679	05-Jan-1988	MINIMAL MASK PROCESS FOR FABRICATING A LATERAL INSULATED GATE SEMI DEVICE
RD 18011		Granted	045494	04-May-1987	4733104	22-Mar-1988	UNIVERSAL INTEGRATED CIRCUIT POWER SUPPLY CHIP
RD 18025P		Granted	048857	12-May-1987	4810617	07-Mar-1989	TREATMENT OF PLANARIZING LAYER IN MULTILAYER ELECTRON BEAM
RD 18163P		Granted	073897	13-Jul-1987	4872039	03-Oct-1989	BURIED LATERAL DIODE AND METHOD FOR MAKING SAME
RD 18171		Granted	178045	05-Apr-1988	4897650	30-Jan-1990	SELF-CHARACTERIZING ANALOG-TO-DIGITAL CONVERTER
RD 18387		Granted	182602	18-Apr-1988	4951221	21-Aug-1990	A CELL STACK FOR VARIABLE DIGIT WIDTH SERIAL ARCHITECTURE
RD 19125		Granted	265285	25-Oct-1988	4895780	23-Jan-1990	ADJUSTABLE WINDAGE METHOD AND MASK FOR CORRECTION OF PROXIM
XRCA71930		Granted	948103	03-Oct-1978	4724530	09-Feb-1988	FIVE TRANSISTOR CMOS MEMORY CELL INCLUDING DIODES
XRCA74253A		Granted	328435	07-Dec-1981	4393438	12-Jul-1983	METHOD FOR THE MANUFACTURE OF PORCELAIN COATED METAL BOARDS

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	FilDate	Pat	IssDate	Title
XRCA75085A		Granted	374967	05-May-1982	4369220	18-Jan-1983	CROSSOVER DIELECTRIC INKS
XRCA75431A		Granted	396662	09-Jul-1982	4399320	16-Aug-1983	CONDUCTOR INKS
XRCA75653B		Granted	780898	27-Sep-1985	4638498	20-Jan-1987	DIGITAL TIMING SYSTEM
XRCA75805A		Granted	396661	09-Jul-1982	4401709	30-Aug-1983	OVERGLAZE INKS
XRCA76785A		Granted	455310	03-Jan-1983	4415624	15-Nov-1983	AIR-FIREABLE THICK FILM INKS
XRCA77188		Granted	363801	31-Mar-1982	4376031	08-Mar-1983	APPARATUS FOR ELECTROPHORETIC DEPOSITION
XRCA77250		Granted	739911	31-May-1985	4651178	17-Mar-1987	DUAL INVERSE ZENER DIODE WITH BURIED JUNCTIONS
XRCA78911		Granted	889209	25-Jul-1986	4731589	15-Mar-1988	CONSTANT CURRENT LOAD AND LEVEL SHIFTER CIRCUITRY
XRCA78956B		Granted	858024	01-May-1986	4652773	24-Mar-1987	INTEGRATED CIRCUITS WITH ELECTRICALLY ERASABLE ELE
XRCA79084		Granted	459754	21-Jan-1983	4467009	21-Aug-1984	INDIUM OXIDE RESISTOR INKS
XRCA79100		Granted	460008	21-Jan-1983	4452844	05-Jun-1984	LOW VALUE RESISTOR INKS
XRCA79245		Granted	685251	21-Dec-1984	4639898	27-Jan-1987	BIT-LINE PULL-UP CIRCUIT
XRCA79643A		Granted	755828	17-Jul-1985	4639752	27-Jan-1987	FAST TERNARY (GAINAS) LOGIC GATE DEVICE
XRCA79815		Granted	612427	21-May-1984	4641261	03-Feb-1987	UNIVERSAL INTERFACE CIRCUIT FOR MICROPROCESSOR PER

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	FilDate	Patent	IssDate	Title
XRCA80702		Granted	674845	26-Nov-1984	4656373	07-Apr-1987	HIGH-SPEED VOLTAGE LEVEL SHIFT CIRCUIT
XRCA81192		Granted	176323	31-Mar-1988	5023613	11-Jun-1991	DECODER ERROR PREVENTION APPARATUS FOR USE IN FLASH ANALOG TO DIGITAL CONVERTERS
XRCA81448		Granted	839917	17-Mar-1986	4682055	21-Jul-1987	A CIRCUIT HAVING ABOUT EQUAL CURRENTS IN COMPLEMEN
XRCA81630		Granted	055220	29-May-1987	4772568	20-Sep-1988	METHOD OF MAKING INTEGRATED CIRCUIT WITH PAIR OF MOS FIELD EFFECT TRANSISTORS SHARE A COMMON SOURCE DRAIN REGION
XRCA81642		Granted	803006	29-Nov-1985	4668080	26-May-1987	METHOD AND APPARATUS FOR FORMING LARGE AREA HIGH R
XRCA81833		Granted	890275	29-Jul-1986	4707623	17-Nov-1987	CMOS INPUT BUFFER CIRCUIT
XRCA81900		Granted	722371	12-Apr-1985	4672314	09-Jun-1987	COMPREHENSIVE SEMICONDUCTOR TEST STRUCTURE
XRCA81971		Granted	777584	19-Sep-1985	4662059	05-May-1987	METHOD OF MAKING STABILIZED SILICON-ON-INSULATOR F
XRCA82183		Granted	055545	29-May-1987	4774452	27-Sep-1988	ZENER REFERENCED VOLTAGE CIRCUIT
XRCA82579		Granted	802020	25-Nov-1985	4702993	27-Oct-1987	MULTILAYER ELECTRON BEAM RESIST
XRCA82756		Granted	166483	10-Mar-1988	4897655	30-Jan-1990	HIGH SPEED APPARATUS FOR A SINGLE LATCH FLASH ANALOG-TO-DIG ITAL CONVERTER
XRCA82787		Granted	823257	28-Jan-1986	4697085	29-Sep-1987	APPARATUS AND METHOD FOR PRODUCING IONS
XRCA82788		Granted	823258	28-Jan-1986	4691109	01-Sep-1987	APPARATUS AND METHOD FOR PRODUCING IONS
XRCA82851		Granted	388416	02-Aug-1989	4923826	08-May-1990	METHOD FOR FORMING DIELECTRICALLY ISOLATED TRANSISTOR

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	Sub Case	Status	Appl	Filedate	Patent	Issuedate	Title
XRCA82865		Granted	359176	31-May-1989	5036219	30-Jul-1991	PRECISE, HIGH SPEED CMOS TRACK (SAMPLE)/HOLD CIRCUITS
XRCA83137		Granted	895365	11-Aug-1986	4794437	27-Dec-1988	ARC GAP FOR INTEGRATED CIRCUITS
XRCA 83180		Granted	173498	25-Mar-1988	4998156	05-Mar-1991	STRUCTURE FOR A COMPLEMENTARY-SYMMETRY COMFET PAIR
XRCA83194		Granted	301073	24-Jan-1989	4945070	31-Jul-1990	METHOD OF MAKING CMOS WITH SHALLOW SOURCE AND DRAIN JUNCTIO NS
XRCA83222		Granted	356086	24-May-1989	4988902	29-Jan-1991	SEMICONDUCTOR TRANSMISSION GATE WITH CAPACITANCE COMPENSATION
XRCA83223		Granted	040168	20-Apr-1987	4968989	06-Nov-1990	SWITCHED CAPACITOR FILTER FOR USE WITH A DIGITAL-TO-ANALOG D/A CONVERTER
XRCA83248		Granted	104405	05-Oct-1987	4783643	08-Nov-1988	IMPEDANCE TRANSFORMING CIRCUIT FOR MULTIBIT PARALLEL DIGITA
XRCA83254		Granted	916846	07-Oct-1986	4737033	12-Apr-1988	ALIGNMENT KEY AND METHOD OF MAKING THE SAME
XRCA83261		Granted	356311	24-May-1989	4978925	18-Dec-1990	UNITY-GAIN CMOS/SOS ZERO-OFFSET BUFFER
XRCA83310		Granted	860814	08-May-1986	4684878	04-Aug-1987	TRANSISTOR BASE CURRENT REGULATOR
XRCA83493		Granted	048704	12-May-1987	4791464	13-Dec-1988	SEMICONDUCTOR DEVICE THAT MINIMIZED THE LEAKAGE CURRENT ASSOCIATED WITH THE PARASITIC EDGE TRANSIS AND A METHOD
XRCA83529		Granted	301926	26-Jan-1989	4945262	31-Jul-1990	VOLTAGE LIMITER APPARATUS WITH INHERENT LEVEL SHIFTING EMPLOYING MOSFETS
XRCA83554		Granted	356084	24-May-1989	5014055	07-May-1991	ANALOG-TO-DIGITAL CONVERTER AND METHOD OF USE UTILIZING CHARGE REDISTRIBUTION
XRCA83563		Granted	120422	13-Nov-1987	4847518	11-Jul-1989	CMOS VOLTAGE DIVIDER CIRCUITS

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	FilDate	Pat	IssDate	Title
XRCA83629		Granted	104406	05-Oct-1987	4833473	23-May-1989	DIGITAL TO ANALOG CONVERTER WITH SWITCH FUNCTION COMPENSATION
XRCA83680		Granted	149514	28-Jan-1988	4924225	08-May-1990	ANALOG TO DIGITAL CONVERTER WITH INTEGRAL LINEARITY ERROR COMPENSATION AND METHOD OF OPERATION
XRCA83871		Granted	084464	12-Aug-1987	4810619	07-Mar-1989	IMPROVED PHOTOLITHOGRAPHY OVER REFLECTIVE SUBSTRATES
XRCA84091		Granted	178982	21-Apr-1988	4967388	30-Oct-1990	TRUNCATED PRODUCT PARTIAL CANONICAL SIGNED DIGIT MULTIPLIER
28-SP-1387		Granted	163534	17-Mar-1988	5015921	14-May-1991	SOFT START SOLID STATE SWITCH
28-SP-1394		Granted	243200	08-Sep-1988	4933994	19-Jun-1990	METHOD FOR FABRICATING A SELF-ALIGNED LIGHTLY DOPED DRAIN SEMICONDUCTOR DEVICE WITH SILICIDE
28-SV-0009		Granted	187869	29-Apr-1988	4947362	07-Aug-1990	DIGITAL FILTER EMPLOYING PARALLEL PROCESSING
28-SV-0018		Granted	440187	22-Nov-1989	5021747	04-Jun-1991	SYMMETRICAL VARIABLE IMPEDANCE APPARATUS EMPLOYING MOS TRANSISTORS
28-SV-0028		Granted	279885	05-Dec-1988	4853610	01-Aug-1989	PRECISION TEMPERATURE-STABLE CURRENT SOURCES/SINKS
28-SV-0035		Granted	390147	07-Aug-1989	4978868	18-Dec-1990	SIMPLIFIED TRANSISTOR BASE CURRENT COMPENSATION CIRCUITRY
28-IS-0063		Granted	07/637047	03-Jan-1991	5150120	22-Sep-1992	MULTIPLEXED SIGMA-DELTA A/D CONVERTER
RD 14706		Granted	534898	22-Sep-1983	4536782	20-Aug-1985	FIELD EFFECT SEMICONDUCTOR DEVICES AND METHOD OF MAKING SAM
RD 12241		Granted	320379	12-Nov-1981	4390393	28-Jun-1983	METHOD OF MAKING INTEGRATED CIRCUITS
RD 13620		Granted	712940	18-Mar-1985	4609932	02-Sep-1986	METHOD FOR FABRICATING NONPLANAR ION-SENSITIVE FIELD-EFFEC

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Client Ref	SubCase	Status	Appl	F Date	Pat	Is Date	Title
RD 13655		Granted	364294	01-Apr-1982	5014102	07-May-1991	MOSFET GATED BIPOLAR TRANSISTORS AND THYRISTORS WITH BOTH TURN ON AND TURN OFF
RD 13683		Granted	387717	11-Jun-1982	4500029	19-Feb-1985	ELECTRICAL ASSEMBLY INCLUDING A CONDUCTOR PATTERN BONDED TO
RD 13870		Granted	395778	06-Jul-1982	4414243	08-Nov-1983	METHOD FOR MAKING SURFACE ACOUSTIC WAVE DEVICE
RD 14037		Granted	333596	23-Dec-1981	4412868	01-Nov-1983	METHOD OF MAKING INTEGRATED CIRCUITS
RD 14111		Granted	394346	01-Jul-1982	4494134	15-Jan-1985	HIGH VOLTAGE SEMICONDUCTOR DEVICES
RD 14133		Granted	616756	04-Jun-1984	4635092	06-Jan-1987	TAPE AUTOMATED MANUFACTURE OF POWER SEMICONDUCTOR DEVICES
RD 14141		Granted	534520	21-Sep-1983	4528582	09-Jul-1985	INTERCONNECTION STRUCTURE FOR POLYCRYSTALLINE SILICON RESIS
RD 14226		Granted	464099	04-Feb-1983	4499558	12-Feb-1985	FIVE TRANSISTOR STATIC MEMORY CELL IMPLEMENTAL IN CMOS/BULK
RD 14227		Granted	478014	23-Mar-1983	4521695	04-Jun-1985	CMOS-D TYPE LARCH EMPLOYING SIX TRANSISTORS AND FOUR DIODES
RD 14230		Granted	478015	23-Mar-1983	4484087	20-Nov-1984	CMOS LATCH CELL INCLUDING FIVE TRANSISTORS AND STATIC FLIP
RD 14504		Granted	471617	03-Mar-1983	4444618	24-Apr-1984	IMPROVED PROCESSES AND GAS MIXTURES FOR THE REACTIVE ION ET
RD 14955		Granted	651014	17-Sep-1984	4628174	09-Dec-1986	FORMING ELECTRICAL CONDUCTORS IN LONG MICRODIAMETER HOLES
RD 15477		Granted	557997	05-Dec-1983	4498924	12-Feb-1985	METHOD FOR PRODUCING EUTECTICS AS THIN FILMS
RD 15478		Granted	557996	05-Dec-1983	4498923	12-Feb-1985	METHOD FOR PRODUCING EUTECTIC AS THIN FILMS

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	CaseStatus	AppNo	FilDate	PatNo	IssDate	Title
RD 15479		Granted	557998	05-Dec-1983	4498925	12-Feb-1985	METHOD FOR PRODUCING EUTECTICS AS THIN FILMS
RD 15480		Granted	557999	05-Nov-1983	4498926	12-Feb-1985	METHOD FOR PRODUCING EUTECTICS AS THIN FILMS
RD 15488		Granted	558123	05-Dec-1983	4496634	29-Jan-1985	EUTECTIC FINE WIRE ARRAYS
RD 15489		Granted	558125	05-Dec-1983	4492739	08-Jan-1985	EUTECTIC FINE WIRE ARRAYS
RD 15490		Granted	558124	05-Dec-1983	4492738	08-Jan-1985	EUTECTIC FINE WIRE ARRAYS
RD 15501		Granted	711333	13-Mar-1985	4583281	22-Apr-1986	METHOD OF MAKING AN INTEGRATED CIRCUIT
RD 15596		Granted	595179	30-Mar-1984	4620258	28-Oct-1986	CIRCUIT FOR SELF COMMUTATED TURN OFF OF LATCHED DEVICES, SU
RD 15805		Granted	667933	02-Nov-1984	4593458	10-Jun-1986	FABRICATION OF INTEGRATED CIRCUIT WITH COMPLEMENTARY DIELEC
RD 16199		Granted	722640	12-Apr-1985	4680603	14-Jul-1987	GRADED EXTENDED DRAIN CONCEPT FOR REDUCED HOT ELECTRON EFFECT
RD 16214		Granted	722642	12-Apr-1985	4613882	23-Sep-1986	HYBRID EXTENDED DRAIN CONCEPT FOR REDUCED HOT ELECTRON EFFE
RD 16232		Granted	803049	29-Nov-1985	4963951	16-Oct-1990	LATERAL INSULATED GATE BIPOLAR TRANSISTORS WITH IMPROVED LATCH UP IMMUNITY
RD 16407		Granted	713215	18-Mar-1985	4597002	24-Jun-1986	FLOW THROUGH ISFET AND METHOD OF FORMING
RD 16483		Granted	840635	17-Mar-1986	4737828	12-Apr-1988	METHOD FOR GATE ELECTRODE FABRICATION AND SYMMETRICAL SELF-
RD 16670		Granted	845110	27-Mar-1986	4767724	30-Aug-1988	UNFRAMED VIA INTERCONNECTION WITH DIELECTRIC ETCH STOP

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRefNo	SubCase	Status	Appl	FilDate	Patent	IssDate	Title
RD 16745		Granted	003678	15-Jan-1987	4796070	03-Jan-1989	LATERAL CHARGE CONTROL SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING
RD 16991		Granted	807612	11-Dec-1985	4862242	29-Aug-1989	SEMICONDUCTOR WAFER WITH AN ELECTRICALLY ISOLATED SEMICONDU
RD 17177		Granted	892652	04-Aug-1986	4729079	01-Mar-1988	ILLUMINATOR FOR VISUAL INSPECTION OF CURVED SPECULAR SURFAC
RD 17190		Granted	868923	29-May-1986	4775952	04-Oct-1988	PROCESS ACCELERATOR
RD 17249		Granted	051427	19-May-1987	4888627	19-Dec-1989	MONOLITHICALLY INTEGRATED LATERAL INSULATED GATE SEMICONDUCTOR DEVICE
RD 17317		Granted	857283	30-Apr-1986	4691433	08-Sep-1987	HYBRID EXTENDED DRAIN CONCEPT FOR REDUCED HOT ELECTRON EFFE
RD 17462		Granted	882857	07-Jul-1986	4778776	18-Oct-1988	PASSIVATION WITH A LOW OXYGEN INTERFACE
RD 17541		Granted	898082	20-Aug-1986	4716124	29-Dec-1987	TAPE AUTOMATED MANUFACTURE OF POWER SEMICONDUCTOR DEVICES
RD 17903P		Granted	041565	23-Apr-1987	4766317	23-Aug-1988	OPTICAL REFLECTANCE METHOD OF EXAMINING A SIMOX ARTICLE
RD 18061P		Granted	093655	08-Sep-1987	4990995	05-Feb-1991	LOW RELFECTANCE CONDUCTOR IN AN INTEGRATED CIRCUIT
RD 18166P		Granted	073371	10-Jul-1987	4733039	22-Mar-1988	METHOD OF LASER SOLDERING
RD 18373P		Granted	124129	23-Nov-1987	4764482	16-Aug-1988	METHOD OF FABRICATING AN INTEGRATED CIRCUIT CONTAINING BIPO
RD 18564		Granted	152703	05-Feb-1988	4868921	19-Sep-1989	HIGH VOLTAGE INTEGRATED CIRCUIT DEVICES ELECTRICALLY INSOLA
RD 18808		Granted	196416	20-May-1988	4859620	22-Aug-1989	GRADED EXTENDED DRAIN CONCEPT FOR REDUCED HOT ELECTRON EFFE

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Client Ref	SubCase	Status	Appl	FiDate	Patent	IssDate	Title
RD 18946		Granted	235087	23-Aug-1988	4908736	13-Mar-1990	SELF PACKAGING CHIP MOUNT
RD 19031		Granted	243210	09-Sep-1988	4942440	17-Jul-1990	HIGH VOLTAGE SEMICONDUCTOR DEVICES WITH REDUCED ON-RESISTAN
RD 19878		Granted	454547	21-Dec-1989	4996116	26-Feb-1991	ENHANCED DIRECT BOND COPPER PROCESS AND STRUCTURE
XRCA78891		Granted	532898	16-Sep-1983	4786814	22-Nov-1988	METHOD OF REDUCING ELECTROSTATIC CHARGE ON ION-IMP
XRCA81354		Granted	935389	26-Nov-1986	4758744	19-Jul-1988	IMPROVED DECODER CIRCUITRY
XRCA83421		Granted	250249	27-Sep-1988	4964726	23-Oct-1990	APPARATUS AND METHOD FOR OPTICAL DIMENSION MEASUREMENT USING INTERFERENCE OF SCATTERED ELECTROMAG ENERGY
28-IS-0043		Granted	757808	22-Jul-1985	4683528	28-Jul-1987	PULSE POSITION MODULATED REGULATION FOR POWER SUPPLIES
28IS00045		Granted	708351	05-Mar-1985	4789959	06-Dec-1988	DELAY CIRCUIT FOR A REAL TIME CLOCK
28-IS-0051		Granted	725216	19-Apr-1985	4754160	28-Jun-1988	POWER SUPPLY SWITCHING CIRCUIT
28-SP-1348		Granted	793426	31-Oct-1985	4750216	07-Jun-1988	VIDEO COUPLER DEVICE
28-SP-1375		Granted	064133	19-Jun-1987	4795716	03-Jan-1989	METHOD OF FABRICATING A POWER IC STRUCTURE
28-SP-1391		Granted	224636	27-Jul-1988	4820968	11-Apr-1989	COMPENSATED CURRENT SENSING CIRCUIT
28-SV-0015		Granted	197098	20-May-1988	4864379	05-Sep-1989	BIPOLAR TRANSISTOR WITH FIELD SHIELDS
35EL01572		Granted	402161	26-Jul-1982	4498172	05-Feb-1985	A SYSTEM FOR POLYDIV SELF TESTING OF DIGITAL NETWORKS

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Client Ref	S/Case	Status	Appl #	Fil Date	Pat #	Iss Date	Title
35EL01652		Granted	450687	17-Dec-1982	4475280	09-Oct-1984	METHOD OF MAKING AN INTEGRATED CIRCUIT INCORPORATING LOW VO
RD 16650		Granted	866648	27-May-1986	4849377	18-Jul-1989	ACTIVE AREA PLANARIZATION WITH SELF ALIGNED CONTACTS
RD 18312		Granted	104002	02-Oct-1987	4824802	25-Apr-1989	METHOD OF FILLING INTERLEVEL DIELECTRIC VIA OR CONTACT HOLES IN MULTILEVEL VLSI METALLIZATION STRUCTURE
RD 19971		Granted	445130	30-Nov-1989	4981816	01-Jan-1991	MO/TI CONTACT TO SILICON
28-SV-0036		Granted	07/456397	26-Dec-1989	4998288	05-Mar-1991	TWO DIMENSIONAL HYBRID DIGITAL CONVOLVER
RD 18404	A	Granted	124393	20-Nov-1987	4809135	28-Feb-1989	IMPROVED CHIP CARRIER AND METHOD OF FABRICATION
RD 19931		Granted	440457	20-Nov-1989	4958210	18-Sep-1990	HIGH VOLTAGE INTEGRATED CIRCUITS
SE-797/796		Granted	07/865868	09-Apr-1992	5504449	02-Apr-1996	POWER DRIVER CIRCUIT
SE-800	A	Granted	08/066697	24-May-1993	5744851	28-Apr-1998	BIASING OF ISLAND-SURROUNDING MATERIAL TO SUPPRESS REDUCTION OF BREAKDOWN VOLTAGE DUE TO FIELD PLATE ACTING ON BURIED LAYER/ISLAND JUNCTION BETWEEN HIGH
SE-801	A	Granted	07/840548	25-Feb-1992	5270569	14-Dec-1993	METHOD AND DEVICE IN WHICH BOTTOMING A WELL IN A DIELECTRICALLY ISOLATED ISLAND IS ASSURED
SE-801	B	Granted	08/091819	13-Jul-1993	5438221	01-Aug-1995	METHOD AND DEVICE IN WHICH BOTTOMING A WELL IN A DIELECTRICALLY ISOLATED ISLAND IS ASSURED
SE-801	C	Granted	08/309573	21-Sep-1994	5602054	11-Feb-1997	METHOD AND DEVICE IN WHICH BOTTOMING A WELL IN A DIELECTRICALLY ISOLATED ISLAND IS ASSURED
SE-799	A	Granted	07/984003	01-Dec-1992	5289336	22-Feb-1994	STATIC ELECTRICITY DISPERSANT
SE-791-LN		Granted	07/840547	25-Feb-1992	5745563	28-Apr-1998	TELEPHONE SUBSCRIBER LINE CIRCUIT, COMPONENTS AND METHODS

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Client Ref	SubCase	Status	Appl	Fil Date	Pat	Iss Date	Title
RD 17837P		Granted	013529	11-Feb-1987	4732838	22-Mar-1988	METHOD OF FORMING A PATTERNED GLASS LAYER OVER THE SURFACE OF A SUBSTRATE
RD 18445P		Granted	134585	14-Dec-1987	4933904	12-Jun-1990	DENSE EPROM AND OPERATING METHODS THEREFOR
RD 19923		Granted	440962	24-Nov-1989	4983537	08-Jan-1991	METHOD OF MAKING A BURRIED OXIDE FIELD ISOLATION STRUCTURE
XRCA80272		Granted	724245	17-Apr-1985	4594560	10-Jun-1986	PRECISION SETTING OF THE BIAS POINT OF AN AMPLIFYI
XRCA80326		Granted	613410	24-May-1984	4639859	27-Jan-1987	PRIORITY ARBITRATION LOGIC FOR A MULT-MASTER BUS S
XRCA80447		Granted	645217	29-Aug-1984	4586375	06-May-1986	REUSABLE CENTRIFUGE FIXTURE AND METHODS OF MAKING
XRCA80515		Granted	631869	18-Jul-1984	4589002	13-May-1986	DIODE STRUCTURE
XRCA80629		Granted	671917	15-Nov-1984	4643385	17-Feb-1987	ANTI-VIBRATION SYSTEM
SE-964		Granted	08/268417	30-Jun-1994	5570407	29-Oct-1996	DISTORTIONLESS X-RAY INSPECTION
SE-967		Granted	08/195667	03-Feb-1994	5451263	19-Sep-1995	PLASMA CLEANING METHOD FOR IMPROVED INK BRAND PERMANENCY ON IC PACKAGES WITH METALLIC PARTS
SE-958		Granted	08/180737	13-Jan-1994	5466963	14-Nov-1995	TRENCH RESISTOR ARCHITECTURE
SE-968		Granted	08/310280	21-Sep-1994	5648678	15-Jul-1997	PROGRAMMABLE ELEMENT IN BARRIER METAL DEVICE AND METHOD
28-SV-0084		Granted	08/180267	12-Jan-1994	5574609	12-Nov-1996	FAIL-SAFE MOS SHUTDOWN CIRCUITRY
SE-1025-TD	A	Granted	08/884032	27-Jun-1997	5808348	15-Sep-1998	NON-UNIFORMLY NITRIDED GATE OXIDE AND METHOD

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

OurClientRef	SubCase	Status	AppNo	AFilDate	Pat	IssDate	Title
SE-1363-TD		Granted	08/929734	15-Sep-1997	6040707	21-Mar-2000	CONSTANT SLEW-RATE AMPLIFIER
SE-1258-AP		Granted	08/931340	16-Sep-1997	5942677	24-Aug-1999	KNOCK SENSOR SYSTEM FOR DETECTING AND RESPONDING TO A DISCONNECT CONDITION (AS AMENDED)
SE-1486-IP		Pending	09/552117	19-Apr-2000			ACCESSING MAIN ATX OUTPUTS WITHOUT MONITORING ALL OUTPUTS
SE-906	D	Pending	09/316580	21-May-1999			BONDED WAFER PROCESSING WITH METAL SILICIDATION
SE-1463-TD		Pending	09/307896	10-May-1999			LASER DECAPSULATION APPARATUS AND METHOD
XRCA72592A		Granted	466593	15-Feb-1983	4433469	28-Feb-1984	METHOD OF FORMING A SELF ALIGNED ALUMINUM POLYCRYS
XRCA72827A		Granted	221367	30-Dec-1980	4668973	26-May-1987	PASSIVATING COMPOSITE FOR A SEMICONDUCTOR DEVICE C
XRCA72827B		Granted	304347	22-Sep-1981	0032351	17-Feb-1987	METHOD OF MANUFACTURING A PASSIVATING COMPOSITE CO
XRCA73341		Granted	335707	30-Dec-1981	4395467	26-Jul-1983	TRANSPARENT CONDUCTIVE FILM HAVING AREAS OF HIGH A
XRCA73678		Granted	320015	10-Nov-1981	4396702	02-Aug-1983	METHOD OF FORMING PATTERN IN POSITIVE RESIST MEDIA
XRCA73760D		Granted	712479	18-Mar-1985	4575746	11-Mar-1986	CROSSUNDERS FOR HIGH DENSITY SOS INTEGRATED CIRCUI
SE-880		Granted	07/947177	18-Sep-1992	5315144	24-May-1994	REDUCTION OF BIPOLAR GAIN AND IMPROVEMENT IN SNAP BACK SUSTAINING VOLTAGE IN SOI FIELD EFFECT TRANSISTOR
SE-883		Granted	07/939115	01-Sep-1992	5270265	14-Dec-1993	STRESS RELIEF TECHNIQUE OF REMOVING OXIDE FROM SURFACE OF TRENCH-PATTERNED SEMICONDUCTOR-ON-INSULATOR STRUCTURE
SE-884/864	A	Granted	08/304433	12-Sep-1994	5548542	20-Aug-1996	HALF BAND FILTER AND METHOD

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	AppNo	FilDate	PatNo	IssDate	Title
SE-884/864	B	Granted	08/462684	05-Jun-1995	5574671	12-Nov-1996	HALF BAND FILTER AND METHOD
SE-891		Granted	07/905015	26-Jun-1992	5311070	10-May-1994	SEU-IMMUNE LATCH FOR GATE ARRAY STANDARD CELL AND OTHER ASIC APPLICATIONS
SE-873		Granted	07/882070	12-May-1992	5322804	21-Jun-1994	INTEGRATION OF HIGH VOLTAGE LATERAL CMOS DEVICES IN LOW VOLTAGE MOS ARCHITECTURE USING CMOS COMPATIBLE PROCESS STEPS
SE-873	A	Granted	08/227157	13-Apr-1994	5541435	30-Jul-1996	INTEGRATION OF HIGH VOLTAGE LATERAL CMOS DEVICES IN LOW VOLTAGE MOS ARCHITECTURE USING CMOS COMPATIBLE PROCESS STEPS
SE-966		Granted	08/462171	05-Jun-1995	5618752	08-Apr-1997	METHOD OF FABRICATION OF SURFACE MOUNTABLE INTEGRATED CIRCUITS
SE-990		Granted	08/456727	01-Jun-1995	5633180	27-May-1997	METHOD OF FORMING P-TYPE ISLANDS OVER P-TYPE BURIED LAYER
SE-996		Granted	08/402381	13-Mar-1995	5659269	19-Aug-1997	ZERO PHASE ERROR SWITCHED-CAPACITOR PHASE LOCKED LOOP FILTER
SE-1002-TL		Granted	08/380409	30-Jan-1995	5671272	23-Sep-1997	CURRENT MODE RING TRIP DETECTOR
SE-1003-TL		Granted	08/380412	30-Jan-1995	5572162	05-Nov-1996	A FILTER WITH REDUCED ELEMENT RATINGS AND METHOD
SE-1004-TD		Granted	08/336768	09-Nov-1994	5643821	01-Jul-1997	METHOD FOR MAKING OHMIC CONTACT TO LIGHTLY DOPED ISLAND FROM A SILICIDE BURIED LAYER AND APPLICATION
XRCA73949		Granted	561220	14-Dec-1983	4727515	23-Feb-1988	HIGH DENSITY PROGRAMMABLE MEMORY ARRAY
XRCA73966		Granted	559720	09-Dec-1983	4499853	19-Feb-1985	DISTRIBUTOR TUBE FOR CVD REACTOR
XRCA74378		Granted	379103	17-May-1982	4420503	13-Dec-1983	LOW TEMPERATURE ELEVATED PRESSURE GLASS FLOW/RE-FL
XRCA74465		Granted	330492	14-Dec-1981	4397938	09-Aug-1983	METHOD OF FORMING RESIST PATTERNS USING X-RAYS OR

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	FiDate	Pat	IssDate	Title
XRCA74518E		Granted	299344	04-Sep-1981	4589008	13-May-1986	APPARATUS FOR ELECTRICALLY JOINING THE ENDS OF SUB
XRCA74727		Granted	412807	30-Aug-1982	4521703	04-Jun-1985	HIGH SPEED SENSE AMPLIFIER
XRCA74823		Granted	304785	23-Sep-1981	4450524	22-May-1984	SINGLE CHIP MICROCOMPUTER WITH EXTERNAL DECODER AN
XRCA74996		Granted	666721	31-Oct-1984	4618849	21-Oct-1986	GRAY CODE COUNTER
XRCA75007		Granted	613415	24-May-1984	4617550	14-Oct-1986	ANALOG-TO-DIGITAL CONVERTERS WITH VIRTUAL INTEGRAT
XRCA75166B		Granted	741703	07-Jun-1985	4595941	17-Jun-1986	PROTECTION CIRCUIT FOR INTEGRATED CIRCUIT DEVICES
XRCA75350		Granted	332831	21-Dec-1981	4489422	18-Dec-1984	FREEZE CLOCK CIRCUIT
XRCA75357A		Granted	380284	20-May-1982	4803528	07-Feb-1989	METHOD FOR FABRICATING ADJACENT CONDUCTING AND INS
XRCA75485		Granted	377001	11-May-1982	4395304	26-Jul-1983	SELECTIVE ETCHING OF PHOSPHOSILICATE GLASS
XRCA75561		Granted	311512	15-Oct-1981	4456837	26-Jun-1984	CIRCUITRY FOR GENERATING NON-OVERLAPPING PULSE TRA
XRCA75596		Granted	510174	01-Jul-1983	4472453	18-Sep-1984	PROCESS FOR RADIATION FREE ELECTRON BEAM DEPOSITIO
XRCA75648A		Granted	561272	14-Dec-1983	4478472	23-Oct-1984	ELECTRICAL CONNECTOR
XRCA75660		Granted	547012	31-Oct-1983	4507334	26-Mar-1985	SURFACE PREPARATION FOR DETERMINING DIFFUSION LENG
XRCA75849		Granted	326162	30-Nov-1981	4449185	15-May-1984	IMPLEMENTATION OF INSTRUCTION FOR A BRANCH WHICH C

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	FilDate	Pat	IssDate	Title
XRCA75868A		Granted	572955	23-Jan-1984	4484331	20-Nov-1984	REGULATOR FOR BIAS CURRENT OF SEMICONDUCTOR LASER
XRCA75902		Granted	646102	31-Aug-1984	4612466	16-Sep-1986	HIGH-SPEED OUTPUT DRIVER
XRCA75915A		Granted	347107	09-Feb-1982	4393160	12-Jul-1983	AQUEOUS DEVELOPABLE POLY(OLEFIN SULFONE) TERPOLYME
XRCA75983		Granted	393616	30-Jun-1982	4496418	29-Jan-1985	PROCESS FOR FORMING AN IMPROVED SILICON-ON-SAPPHIR
XRCA75992		Granted	328437	07-Dec-1981	4434381	28-Feb-1984	SENSE AMPLIFIERS
XRCA76011		Granted	390782	21-Jun-1982	4445270	01-May-1984	LOW RESISTANCE CONTACT FOR HIGH DENSITY INTEGRATED
XRCA76041		Granted	362465	26-Mar-1982	4450562	22-May-1984	TWO LEVEL PARITY ERROR CORRECTION SYSTEM
XRCA76166		Granted	448724	10-Dec-1982	4716451	29-Dec-1987	SEMICONDUCTOR DEVICE WITH INTERNAL GETTERING REGION
XRCA76204		Granted	349515	17-Feb-1982	4498775	12-Feb-1985	METHOD FOR DETECTING DISTANCE DEVIATIONS TO A PHOT
XRCA76218A		Granted	480596	30-Mar-1983	4495427	22-Jan-1985	PROGRAMMABLE LOGIC GATES AND NETWORKS
XRCA76543		Granted	359434	18-Mar-1982	4450371	22-May-1984	SPEED UP CIRCUIT
XRCA76692		Granted	560459	12-Dec-1983	4519126	28-May-1985	METHOD OF FABRICATING HIGH SPEED CMOS DEVICES
XRCA76700A		Granted	396663	09-Jul-1982	4405776	20-Sep-1983	POSITIVE RADIATION SENSITIVE RESIST TERPOLYMER FRO
XRCA76859		Granted	334818	28-Dec-1981	4441069	03-Apr-1984	SELF-EXTINGUISHING LOAD DRIVING SYSTEM

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Client Ref	SubCase	Status	US Apl	FilDate	US Pat	IssDate	Title
XRCA76972		Granted	313660	22-Oct-1981	4437024	13-Mar-1984	ACTIVELY CONTROLLED INPUT BUFFER
XRCA76998		Granted	326153	30-Nov-1981	4449118	15-May-1984	SWITCHING CIRCUITRY AS FOR A FLASH A/D CONVERTER
XRCA77148		Granted	322002	16-Nov-1981	4460868	17-Jul-1984	FIXTURE FOR TESTING SEMICONDUCTOR DEVICES
XRCA77193		Granted	444164	24-Nov-1982	4502014	26-Feb-1985	COINCIDENT PULSE CANCELLING CIRCUIT
XRCA77199		Granted	362464	26-Mar-1982	4472805	18-Sep-1984	MEMORY SYSTEM WITH ERROR STORAGE
XRCA77238		Granted	582752	23-Feb-1984	4512073	23-Apr-1985	METHOD OF FORMING SELF-ALIGNED CONTACT OPENINGS
XRCA77251		Granted	421517	22-Sep-1982	4484244	20-Nov-1984	PROTECTION CIRCUIT FOR INTEGRATED CIRCUIT DEVICES
XRCA77256		Granted	376572	10-May-1982	4436509	13-Mar-1984	CONTROLLED ENVIRONMENT FOR DIFFUSION FURNACE
XRCA77321		Granted	335852	30-Dec-1981	4357203	02-Nov-1982	PLASMA ETCHING OF POLYIMIDE
XRCA77339		Granted	479518	28-Mar-1983	4457976	03-Jul-1984	METHOD FOR MOUNTING A SAPPHIRE CHIP ON A METAL BAS
XRCA77403		Granted	342473	25-Jan-1982	4439245	27-Mar-1984	ELECTROMAGNETIC RADIATION ANNEALING OF SEMICONDUCT
XRCA77450		Granted	547326	31-Oct-1983	4567431	28-Jan-1986	METHOD FOR REVEALING SEMICONDUCTOR SURFACE DAMAGE
XRCA77461		Granted	330579	14-Dec-1981	4397939	09-Aug-1983	METHOD OF USING A POSITIVE ELECTRON BEAM RESIST ME
XRCA77474		Granted	352179	25-Feb-1982	4442409	10-Apr-1984	PUSH-PULL NON-COMPLEMENTARY TRANSISTOR AMPLIFIER

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	FiDate	Pat	IssDate	Title
XRCA77496		Granted	352883	26-Feb-1982	4482422	13-Nov-1984	METHOD FOR GROWING A LOW DEFECT MONOCRYSTALLINE LA
XRCA77524		Granted	362041	25-Mar-1982	4372807	08-Feb-1983	PLASMA ETCHING OF ALUMINUM
XRCA77525		Granted	362044	25-Mar-1982	4375385	01-Mar-1983	PLASMA ETCHING OF ALUMINUM
XRCA77557		Granted	320434	12-Nov-1981	4429283	31-Jan-1984	DIFFERENTIAL CURRENT AMPLIFIER
XRCA77561		Granted	362043	25-Mar-1982	4370196	25-Jan-1983	ANISOTROPIC ETCHING OF ALUMINUM
XRCA77565		Granted	448690	10-Dec-1982	4513397	23-Apr-1985	ELECTRICALLY ALTERABLE, NONVOLATILE FLOATING GATE
XRCA77663		Granted	571423	17-Jan-1984	4582745	15-Apr-1986	DIELECTRIC LAYERS IN MULTILAYER REFRACTORY METALLI
XRCA77676		Granted	565338	27-Dec-1983	4470871	11-Sep-1984	PREPARATION OF ORGANIC LAYERS FOR OXYGEN ETCHING
XRCA77679		Granted	320016	10-Nov-1981	4357369	02-Nov-1982	METHOD OF PLASMA ETCHING A SUBSTRATE
XRCA77895		Granted	401625	26-Jul-1982	4471243	11-Sep-1984	BIDIRECTIONAL INTERFACE
XRCA77920		Granted	391923	24-Jun-1982	4401775	30-Aug-1983	EPOXY ENCAPSULATING FORMULATION
XRCA77961		Granted	476781	18-Mar-1983	4442134	10-Apr-1984	CHEMICAL DEPOSITION TERMINATION
XRCA77965A		Granted	793311	31-Oct-1985	4642772	10-Feb-1987	SYSTEM FOR DETERMINING TIME DURATION OF ANGULAR RO
XRCA78024		Granted	435971	22-Oct-1982	4440799	03-Apr-1984	MONITOR FOR IMPURITY LEVELS IN ALUMINUM DEPOSITION

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl #	FiDate	Pat #	IssDate	Title
XRCA78078		Granted	605245	30-Apr-1984	4625120	25-Nov-1986	DEEP ULTRAVIOLET (DUV) FLOOD EXPOSURE SYSTEM
XRCA78128		Granted	362463	26-Mar-1982	4464755	07-Aug-1984	MEMORY SYSTEM WITH ERROR DETECTION AND CORRECTION
XRCA78129		Granted	362462	26-Mar-1982	4464754	07-Aug-1984	MEMORY SYSTEM WITH REDUNDANCY FOR ERROR AVOIDANCE
XRCA78160		Granted	567336	30-Dec-1983	4546487	08-Oct-1985	AUTO RANGING COUNTER
XRCA78254		Granted	405451	05-Aug-1982	4487125	11-Dec-1984	TIMING CIRCUIT
XRCA78299		Granted	437835	29-Oct-1982	4451507	29-May-1984	AUTOMATIC LIQUID DISPENSING APPARATUS FOR SPINNING
XRCA78324		Granted	439562	05-Nov-1982	4498772	12-Feb-1985	METHOD TO DETERMINE THE CRYSTALLINE PROPERTIES OF
XRCA78341		Granted	537817	30-Sep-1983	4532436	30-Jul-1985	FAST SWITCHING CIRCUIT
XRCA78360		Granted	386240	08-Jun-1982	4436999	13-Mar-1984	STRUCTURAL DEFECT DETECTION
XRCA78366		Granted	563627	20-Dec-1983	4612211	16-Sep-1986	SELECTIVE SEMICONDUCTOR COATING AND PROTECTIVE MAS
XRCA78374		Granted	381733	24-May-1982	4462002	24-Jul-1984	TRIMMING CIRCUITS FOR PRECISION AMPLIFIER
XRCA78386		Granted	380289	20-May-1982	4491807	01-Jan-1985	FET NEGATIVE RESISTANCE CIRCUITS
XRCA78463		Granted	484525	13-Apr-1983	4476994	16-Oct-1984	LID LATCHING APPARATUS
XRCA78468		Granted	483876	11-Apr-1983	4421593	20-Dec-1983	REVERSE ETCHING OF CHROMIUM

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Client Ref	SubCase	Ex Status	Ex Appl	Ex Filed	Ex Pat	Ex Issued	Ex Title
XRCA78469		Granted	441682	15-Nov-1982	4433044	21-Feb-1984	DRY DEVELOPABLE POSITIVE PHOTORESISTS
XRCA78554		Granted	456493	07-Jan-1983	4472210	18-Sep-1984	METHOD OF MAKING A SEMICONDUCTOR DEVICE TO IMPROVE
XRCA78607		Granted	450062	15-Dec-1982	4525635	25-Jun-1985	TRANSIENT SIGNAL SUPPRESSION CIRCUIT
XRCA78660		Granted	407897	13-Aug-1982	4471237	11-Sep-1984	OUTPUT PROTECTION CIRCUIT FOR PREVENTING A REVERSE
XRCA78665		Granted	448279	09-Dec-1982	4411734	25-Oct-1983	ETCHING OF TANTALUM SILICIDE/DOPED POLYSILICON STR
XRCA78705		Granted	532973	16-Sep-1983	4489103	18-Dec-1984	SIPOS DEPOSITION METHOD
XRCA78707		Granted	451818	21-Dec-1982	4400257	23-Aug-1983	METHOD OF FORMING METAL LINES
XRCA78784A		Granted	783268	04-Oct-1985	4579454	01-Apr-1986	OPTICAL PROFILOMETER FOR STEEP SURFACE CONTOURS WI
XRCA78807		Granted	509787	30-Jun-1983	4567387	28-Jan-1986	LINEAR SENSE AMPLIFIER
XRCA78808		Granted	528035	31-Aug-1983	4639897	27-Jan-1987	PRIORITY ENCODED SPARE ELEMENT DECODER
XRCA78837		Granted	457578	13-Jan-1983	4686112	11-Aug-1987	DEPOSITION OF SILICON DIOXIDE
XRCA78840		Granted	444459	24-Nov-1982	4501978	26-Feb-1985	LEVEL SHIFT INTERFACE CIRCUIT
XRCA78877		Granted	499397	31-May-1983	4558435	10-Dec-1985	MEMORY SYSTEM
XRCA78890		Granted	532899	16-Sep-1983	4560879	24-Dec-1985	METHOD AND APPARATUS FOR IMPLANTATION OF DOUBLY-CH

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

CaseRef	SubCase	Status	Appl	FilDate	Patn	IssDate	Title
XRCA78892A		Granted	775942	12-Sep-1985	4595837	17-Jun-1986	METHOD FOR PREVENTING ARCING IN A DEVICE DURING IO
XRCA78902		Granted	764551	12-Aug-1985	4660276	28-Apr-1987	METHOD OF MAKING AN MOS FIELD EFFECT TRANSISTOR IN
XRCA78945A		Granted	715039	22-Mar-1985	4598462	08-Jul-1986	METHOD FOR MAKING SEMICONDUCTOR DEVICE WITH INTEGR
XRCA78956Z		Granted	627920	05-Jul-1984	4596938	24-Jun-1986	ELECTRICALLY ERASABLE PROGRAMMABLE ELECTRONIC CIRC
XRCA79011		Granted	523921	17-Aug-1983	4608591	26-Aug-1986	ELECTRICALLY ALTERABLE PROGRAMMABLE NONVOLATILE FL
XRCA79016		Granted	633188	23-Jul-1984	4618876	21-Oct-1986	ELECTRICALLY ALTERABLE, NONVOLATILE FLOATING GATE
XRCA79086		Granted	443925	23-Nov-1982	4529892	16-Jul-1985	DETECTION CIRCUITRY WITH MULTIPLE OVERLAPPING THRE
XRCA79112		Granted	828687	12-Feb-1986	4926236	15-May-1990	MULTILAYER INTERCONNECT AND METHOD OF FORMING SAME
XRCA79157		Granted	475035	14-Mar-1983	4457259	03-Jul-1984	APPARATUS FOR SPRAYING A LIQUID ON A SPINNING SURF
XRCA79196		Granted	546181	27-Oct-1983	4558345	10-Dec-1985	MULTIPLE CONNECTION BOND PAD FOR AN INTEGRATED CIR
XRCA79221		Granted	728588	29-Apr-1985	4603082	29-Jul-1986	DIAMOND-LIKE FILM
XRCA79518		Granted	556931	01-Dec-1983	4567381	28-Jan-1986	BIAS NETWORK HAVING ONE MODE FOR PRODUCING A REGUL
XRCA79556		Granted	584814	29-Feb-1984	4598249	01-Jul-1986	METHOD USING SURFACE PHOTOVOLTAGE (SPV) MEASUREMEN
XRCA79558		Granted	553255	18-Nov-1983	4502206	05-Mar-1985	METHOD OF FORMING SEMICONDUCTOR CONTACTS BY IMPLAN

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Ty Status	Ap	FiDate	Pat	IssDate	Title
XRCA79563		Granted	605244	30-Apr-1984	4575636	11-Mar-1986	DEEP ULTRAVIOLET (DUV) FLOOD EXPOSURE SYSTEM
XRCA79679		Granted	592397	22-Mar-1984	4504521	12-Mar-1985	LPCVD DEPOSITION OF TANTALUM SILICIDE
XRCA79754		Granted	562529	19-Dec-1983	4631422	23-Dec-1986	TTL CIRCUIT WITH A CLAMPING TRANSISTOR FOR SPEEDY
XRCA79829		Granted	503044	10-Jun-1983	4566025	21-Jan-1986	CMOS STRUCTURE INCORPORATING VERTICAL IGFETS
XRCA79885		Granted	710271	11-Mar-1985	4633283	30-Dec-1986	CIRCUIT AND STRUCTURE FOR PROTECTING INTEGRATED CIRCUITS FROM DESTRUCTIVE TRANSIENT VOLTAGES
XRCA79944		Granted	634397	25-Jul-1984	4584026	22-Apr-1986	ION-IMPLANTATION OF PHOSPHORUS, ARSENIC OR BORON B
XRCA80087		Granted	717827	29-Mar-1985	4641130	03-Feb-1987	ANALOG-TO-DIGITAL CONVERTER WITH SCALING OF INPUT
XRCA80205		Granted	562530	19-Dec-1983	4460435	17-Jul-1984	PATTERNING OF SUBMICROMETER METAL SILICIDE STRUCTU
XRCA80221		Granted	755012	15-Jul-1985	4689575	25-Aug-1987	CLOCK SYNCHRONIZATION CIRCUIT FOR A COMPUTER TIMER
XRCA80760A		Granted	940167	10-Dec-1986	4947221	07-Aug-1990	MEMORY CELL FOR A DENSE EPROM
XRCA80765		Granted	609360	11-May-1984	4614897	30-Sep-1986	SWITCHING CIRCUIT
XRCA80768		Granted	778986	23-Sep-1985	4637836	20-Jan-1987	PROFILE CONTROL OF BORON IMPLANT
XRCA80776		Granted	625910	29-Jun-1984	4648074	03-Mar-1987	REFERENCE CIRCUIT WITH SEMICONDUCTOR MEMORY ARRAY
XRCA80777		Granted	628302	06-Jul-1984	4594518	10-Jun-1986	VOLTAGE LEVEL SENSING CIRCUIT

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	FilDate	Pat	IssDate	Title
XRCA80794		Granted	809132	16-Dec-1985	4695744	22-Sep-1987	LEVEL SHIFT CIRCUIT
XRCA80885		Granted	687366	28-Dec-1984	4576829	18-Mar-1986	LOW TEMPERATURE GROWTH OF SILICON DIOXIDE ON SILIC
XRCA80960		Granted	748350	24-Jun-1985	4605479	12-Aug-1986	IN-SITU CLEANED OHMIC CONTACTS
XRCA81246		Granted	655692	28-Sep-1984	4547261	15-Oct-1985	ANISOTROPIC ETCHING OF ALUMINUM
XRCA81287		Granted	766285	16-Aug-1985	4621042	04-Nov-1986	ABSORPTIVE PLANARIZING LAYER FOR OPTICAL LITHOGRAP
XRCA81366		Granted	852289	15-Apr-1986	4735919	05-Apr-1988	METHOD OF MAKING A FLOATING GATE MEMORY CELL
XRCA81381		Granted	636832	06-Aug-1984	4546016	08-Oct-1985	DEPOSITION OF BOROPHOSPHOSILICATE GLASS
XRCA81526A		Granted	885744	21-Jul-1986	4684970	04-Aug-1987	HIGH CURRENT LATERAL TRANSISTOR STRUCTURE
XRCA81549		Granted	710284	11-Mar-1985	4585515	29-Apr-1986	FORMATION OF CONDUCTIVE LINES
XRCA81555		Granted	793237	31-Oct-1985	4613829	23-Sep-1986	SWITCHABLE OSCILLATOR CIRCUIT
XRCA81632		Granted	694100	23-Jan-1985	4592792	03-Jun-1986	METHOD FOR FORMING UNIFORMLY THICK SELECTIVE EPITA
XRCA81773		Granted	748355	24-Jun-1985	4609614	02-Sep-1986	PROCESS OF USING ABSORPTIVE LAYER IN OPTICAL LITHO
XRCA81793		Granted	702338	15-Feb-1985	4608118	26-Aug-1986	REACTIVE SPUTTER ETCHING OF METAL SILICIDE STRUCTU
XRCA81824		Granted	711720	14-Mar-1985	4612270	16-Sep-1986	TWO-LAYER NEGATIVE RESIST

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Client Ref	Sub Case	Status	Appl No	Filing Date	Patent No	Issue Date	Title
XRCA81830		Granted	833074	26-Feb-1986	4792837	20-Dec-1988	ORTHOGONAL BIPOLAR TRANSISTOR
XRCA81884		Granted	741358	05-Jun-1985	4618565	21-Oct-1986	ABSORPTIVE LAYER FOR OPTICAL LITHOGRAPHY
XRCA81976		Granted	755915	17-Jul-1985	4620366	04-Nov-1986	AUTOMATIC PIN EXTRACTION APPARATUS FOR INTEGRATED
XRCA82016		Granted	729165	30-Apr-1985	4615762	07-Oct-1986	METHOD FOR THINNING SILICON
XRCA82091		Granted	792535	29-Oct-1985	4741926	03-May-1988	SPIN-COATING PROCEDURE
XRCA82163		Granted	739820	31-May-1985	4631562	23-Dec-1986	ZENER DIODE STRUCTURE
XRCA82199		Granted	857154	29-Apr-1986	4685199	11-Aug-1987	METHOD FOR FORMING DIELECTRICALLY ISOLATED PMOS, N
XRCA82251A		Granted	148209	22-Jan-1988	4881010	14-Nov-1989	ION IMPLANTATION METHOD AND APPARATUS
XRCA82287		Granted	891170	31-Jul-1986	4741212	03-May-1988	METHOD FOR DETERMINING STRUCTURAL DEFECTS IN SEMIC
XRCA82355		Granted	792473	29-Oct-1985	4614294	30-Sep-1986	APPARATUS FOR HOLDING A PART IN A WAVE SOLDERING M
XRCA82389A		Granted	905077	09-Sep-1986	4784936	15-Nov-1988	PROCESS OF FORMING A RESIST STRUCTURE
XRCA82410		Granted	792790	30-Oct-1985	4687730	18-Aug-1987	LIFT-OFF TECHNIQUE FOR SUB-MICROMETER LITHOGRAPHY
XRCA82427		Granted	762521	05-Aug-1985	4662064	05-May-1987	METHOD OF FORMING MULTI-LEVEL METALLIZATION
XRCA82468		Granted	852290	15-Apr-1986	4687537	18-Aug-1987	EPITAXIAL METAL SILICIDE LAYERS

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	Subcase	Status	Appl	FiDate	Pat	IssDate	Title
XRCA82522		Granted	878259	25-Jun-1986	4692992	15-Sep-1987	METHOD OF FORMING ISOLATION REGIONS IN A SEMICONDUCTOR DEVI CE
XRCA82533		Granted	799825	20-Nov-1985	4789889	06-Dec-1988	INTEGRATED CIRCUIT DEVICE HAVING SLANTED PERIPHERA
XRCA82741		Granted	802994	29-Nov-1985	4698316	06-Oct-1987	METHOD OF DEPOSITING UNIFORMLY THICK SELECTIVE EPI
XRCA83023		Granted	820808	22-Jan-1986	4779161	18-Oct-1988	MULTI-DRIVER INTEGRATED CIRCUIT
XRCA83024		Granted	885165	14-Jul-1986	4710440	01-Dec-1987	TEST MASK FOR DETERMINING ALIGNMENT OF AN AUTOMATI
XRCA83058		Granted	880031	30-Jun-1986	4722654	02-Feb-1988	ARTICLE TRANSFER SYSTEM
XRCA83074		Granted	834386	28-Feb-1986	4654545	31-Mar-1987	OVERVOLTAGE COMPARATOR
XRCA83075		Granted	834387	28-Feb-1986	4680483	14-Jul-1987	COMPARATOR CIRCUIT
XRCA83114		Granted	834385	28-Feb-1986	4786961	22-Nov-1988	BIPOLAR TRANSISTOR WITH TRANSIENT SUPPRESSOR
XRCA83208		Granted	925982	03-Nov-1986	4695922	22-Sep-1987	CONSTANT RATIO, SIZE INSENSITIVE, CAPACITOR STRUCT
XRCA83325		Granted	298148	18-Jan-1989	4897366	30-Jan-1990	METHOD OF MAKING SILICON-ON-INSULATOR ISLANDS
XRCA83355		Granted	856277	28-Apr-1986	4722912	02-Feb-1988	METHOD OF FORMING A SEMICONDUCTOR STRUCTURE
XRCA83405		Granted	015478	17-Feb-1987	4731695	15-Mar-1988	CAPACITOR AND METHOD FOR MAKING SAME WITH HIGH YIE
XRCA83805		Granted	913325	30-Sep-1986	4698132	06-Oct-1987	METHOD OF FORMING TAPERED CONTACT OPENINGS

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Client Ref	SubCase	Status	Appl No	Fil Date	Pat No	Iss Date	Title
XRCA83806		Granted	007858	28-Jan-1987	4710261	01-Dec-1987	APPARATUS AND METHOD FOR MAINTAINING A UNIFORM ETCHING SOLUTION COMPOSITION
XRCA83868A		Granted	418762	06-Oct-1989	4927777	22-May-1990	METHOD OF MAKING AN MOS TRANSISTOR
XRCA83895		Granted	306356	06-Feb-1989	5053345	01-Oct-1991	METHOD OF EDGE DOPING SOI ISLANDS
XRCA84087		Granted	07/278400	01-Dec-1988	5003615	26-Mar-1991	OPTOELECTRONIC SYSTEM FOR DETERMINING SURFACE IRREGULARITIES OF A WORKPIECE HAVING A NOMINALLY PLANE REFLECTIVE SURFACE
XRCA83775		Granted	243367	12-Sep-1988	4872141	03-Oct-1989	RADIATION HARD MEMORY CELL HAVING NONOCRYSTALLINE AND NONO MONOCRYSTALLINE INVERTERS AND METHOD FOR MAKING SAME
XRCA83854		Granted	904271	05-Sep-1986	4989061	29-Jan-1991	RADIATION HARD MEMORY CELL STRUCTURE WITH DRAIN SHIELDING
XRCA83471		Granted	900520	26-Aug-1986	4833644	23-May-1989	MEMORY CELL CIRCUIT HAVING RADIATION HARDNESS
RD 18539		Granted	151045	01-Feb-1988	4933742	12-Jun-1990	METALLIZATION CONTACT SYSTEM FOR LARGE SCALE INTEGRATED CIRCUITS
RD 19325		Granted	312849	17-Feb-1989	4914812	10-Apr-1990	SELF PACKAGING CHIP MOUNT
SE-807		Granted	07/791853	14-Nov-1991	5220868	22-Jun-1993	PRINT BAND CLEANER
28-IS-0066		Granted	07/720082	24-Jun-1991	5332931	26-Jul-1994	HIGH SPEED DIFFERENTIAL COMPARATOR
28-IS-0066	A	Granted	08/018619	17-Feb-1993	5329187	12-Jul-1994	HIGH SPEED DIFFERENTIAL COMPARATOR
28-SP-1397		Granted	07/663224	01-Mar-1991	5105099	14-Apr-1992	LEVEL SHIFT CIRCUIT WITH COMMON MODE REJECTION
28-SV-0045		Granted	07/696481	06-May-1991	5142244	25-Aug-1992	FULL RANGE INPUT/OUTPUT COMPARATOR

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	Subcase	Status	Appl	FilDate	Pat	IssDate	Title
28-SV-0062		Granted	07/682482	09-Apr-1991	5196737	23-Mar-1993	LATCHING COMPARATOR EMPLOYING TRANSFER GATES
28-SV-0067		Granted	07/716488	17-Jun-1991	5335132	02-Aug-1994	OVER-VOLTAGE SENSOR WITH HYSTERESIS
RD 20002P		Granted	453090	22-Dec-1989	4999691	12-Mar-1991	IC WITH STACKED MOS FIELD EFFECT TRANSISTORS AND METHODS OF MAKING SAME
28-SV-0072		Granted	07/667932	12-Mar-1991	5130569	14-Jul-1992	POWER-ON RESET CIRCUIT
SE-814		Granted	07/791856	14-Nov-1991	5302859	12-Apr-1994	SYMMETRIC, HIGH SPEED, VOLTAGE SWITCHING CIRCUIT POSSESSING REVERSE VOLTAGE APPLICATION IMMUNITY
SE-848		Granted	07/806074	11-Dec-1991	5229661	20-Jul-1993	HI SPEED BIPOLAR DIGITAL LOGIC GATE ARCHITECTURE
SE-856		Granted	07/854805	19-Mar-1982	5217919	08-Jun-1993	METHOD OF FORMING ISLAND WITH POLYSILICON FILLED TRENCH ISOLATION
SE-860		Granted	07/904848	26-Jun-1992	5300877	05-Apr-1994	PRECISION VOLTAGE REFERENCE CIRCUIT
SE-816		Granted	07/785395	25-Oct-1991	5382916	17-Jan-1995	DIFFERENTIAL VOLTAGE FOLLOWER
SE-816	A	Granted	08/287763	09-Aug-1994	5471131	28-Nov-1995	DIFFERENTIAL VOLTAGE FOLLOWER
SE-822-SP		Granted	07/785325	30-Oct-1991	5369309	29-Nov-1994	ANALOG-TO-DIGITAL CONVERTER AND METHOD OF FABRICATION
SE-822-SP	C	Granted	08/571693	13-Dec-1995	5631599	20-May-1997	ANALOG-TO-DIGITAL CONVERTER AND METHOD OF FABRICATION
SE-823	B	Granted	08/391490	21-Feb-1995	5481129	02-Jan-1996	ANALOG-TO-DIGITAL CONVERTER
RD 18406		Granted	121183	16-Nov-1987	4845050	04-Jul-1989	OHMIC CONTACTS AND INTERCONNECTS TO SILICON AND METHOD OF MAKING THE SAME

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	US Status	US Appl	US Filedate	US Pat	US Issdate	Title
RD 18903P		Granted	218425	12-Jul-1988	4903094	20-Feb-1990	MEMORY CELL STRUCTURE HAVING RADIATION HARDNESS
RD 19030		Granted	246068	16-Sep-1988	4903107	20-Feb-1990	METHOD OF MAKING A BURIED OXIDE FIELD INSULATION STRUCTURE
RD 17387		Granted	866530	23-May-1986	4737217	12-Apr-1988	A SUBSTRATE FORA SEMICONDUCTOR CHIP PACKAGE AND A METHOD OF FABRICATING THE SAME
SE-862/870		Granted	07/832694	06-Feb-1992	5298434	29-Mar-1994	SELECTIVE RECRYSTALLIZATION TO REDUCE P-CHANNEL TRANSISTOR LEAKAGE IN SILICON-ON-SAPPHIRE CMOS RADIATION HARDENED IC's.
SE-862/870	A	Granted	08/171280	21-Dec-1993	5391903	21-Feb-1995	SELECTIVE RECRYSTALLIZATION TO REDUCE P-CHANNEL TRANSISTOR LEAKAGE IN SILICON-ON-SAPPHIRE CMOS RADIATION HARDENED IC's.
28-SV-0071		Granted	07/781626	24-Oct-1991	5262689	16-Nov-1993	BIMOS CURRENT DRIVER CIRCUIT
28-SV-0065		Granted	07/846286	03-Mar-1992	5640346	17-Jun-1997	ELECTRICALLY PROGRAMMABLE MEMORY CELL
SE-861		Granted	07/831252	23-Dec-1991	5434357	18-Jul-1995	REDUCED SEMICONDUCTOR SIZE PACKAGE
SE-877		Granted	07/855834	23-Mar-1992	5293052	08-Mar-1994	SOI CMOS DEVICE HAVING DIFFERENTIALLY DOPED BODY EXTENSION FOR PROVIDING IMPROVED BACKSIDE LEAKAGE CHANNEL STOP
SE-852		Granted	07/839426	20-Feb-1992	5228330	20-Jul-1993	HERMETIC IC PACKAGE MOISTURE TESTER
SE-826		Granted	07/917635	20-Jul-1992	5856695	05-Jan-1999	BICMOS DEVICES
RD 19963		Granted	07/603495	26-Oct-1990	5184206	02-Feb-1993	DIRECT THERMOCOMPRESSION BONDING TECHNOLOGY FOR THIN ELECTRONIC POWER CHIP PACKAGES
RD 19963	A	Granted	07/950553	25-Sep-1992	5206186	27-Apr-1993	DIRECT THERMOCOMPRESSION BONDING TECHNOLOGY FOR THIN ELECTRONIC POWER CHIP PACKAGES
RD 19963	B	Granted	08/007300	21-Jan-1993	5304847	19-Apr-1994	DIRECT THERMOCOMPRESSION BONDING TECHNOLOGY FOR THIN ELECTRONIC POWER CHIP PACKAGES

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Client Ref	SubCase	St Status	Appl #	Filing Date	Pat #	Issue Date	Title
RD 20108		Granted	07/632876	24-Dec-1990	5418002	23-May-1995	DIRECT BONDING OF COPPER TO ALUMINUM NITRIDE SUBSTRATES
SE-873	B	Granted	08/474647	07-Jun-1995	5622878	22-Apr-1997	INTEGRATION OF HIGH VOLTAGE LATERAL CMOS DEVICES IN LOW VOLTAGE MOS ARCHITECTURE USING CMOS COMPATIBLE PROCESS STEPS
SE-898/900		Granted	07/921197	28-Jul-1992	5362667	08-Nov-1994	BONDED WAFER PROCESSING
SE-898/900	A	Granted	08/287773	09-Aug-1994	5517047	14-May-1996	BONDED WAFER PROCESSING
SE-898/900	B	Granted	08/573551	15-Dec-1995	5728624	17-Mar-1998	BONDED WAFER PROCESSING
SE-894		Granted	07/935765	26-Aug-1992	5382541	17-Jan-1995	METHOD FOR FORMING RECESSED OXIDE ISOLATION CONTAINING DEEP AND SHALLOW TRENCHES
SE-894	A	Granted	08/339966	15-Nov-1994	5504033	02-Apr-1996	METHOD FOR FORMING RECESSED OXIDE ISOLATION CONTAINING DEEP AND SHALLOW TRENCHES
SE-872		Granted	07/925077	05-Aug-1992	5338960	16-Aug-1994	FORMATION OF DUAL POLARITY SOURCE/DRAIN EXTENSIONS IN LATERAL COMPLEMENTARY CHANNEL MOS ARCHITECTURES
SE-895		Granted	07/913844	14-Jul-1992	5279850	18-Jan-1994	GAS PHASE CHEMICAL REDUCTION OF METALLIC BRANDING LAYER OF ELECTRONIC CIRCUIT PACKAGE FOR DEPOSITION OF BRANDING INK
SE-865		Granted	07/930926	14-Aug-1992	5276633	04-Jan-1994	SINE/COSINE GENERATOR AND METHOD
SE-865	A	Granted	08/400811	08-Mar-1995	RE36388	09-Nov-1999	SINE/COSINE GENERATOR AND METHOD
SE-876		Granted	07/930169	14-Aug-1992	5455782	03-Oct-1995	A DIGITAL DECIMATING FILTER WITH VIRTUAL REGISTER SPACE AND VARIABLE DECIMATION RATES
SE-887		Granted	07/911902	10-Jul-1992	5352327	04-Oct-1994	REDUCED TEMPERATURE SUPPRESSION OF VOLATILIZATION OF PHOTOEXCITED HALOGEN REACT PRODUCTS FROM SILICON WAFER
28-SV-0027		Granted	07/935830	26-Aug-1992	5334929	02-Aug-1994	CIRCUIT FOR PROVIDING A CURRENT PROPORTIONAL TO ABSOLUTE TEMPERATURE

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	Subcase	Status	Appl	Fildate	Pat	Issdate	Title
28-SV-0058		Granted	07/936596	27-Aug-1992	5287068	15-Feb-1994	COMPARATOR AMPLIFIER
28-SV-0061		Granted	07/962309	16-Oct-1992	5307023	26-Apr-1994	IMPROVED NON-LINEAR OTA
RD 21590	A	Granted	07/777495	15-Oct-1991	5100740	31-Mar-1992	DIRECT BONDED SYMMETRIC-METALLIC-LAMINATE/SUBSTRATE STRUCTURES
28-SV-0079		Granted	07/941736	08-Sep-1992	5347169	13-Sep-1994	INDUCTIVE LOAD DUMP CIRCUIT
SE-907	A	Granted	08/430312	28-Apr-1995	5849627	15-Dec-1998	BONDED WAFER PROCESSING WITH OXIDATIVE BONDING
SE-912		Granted	07/930737	14-Aug-1992	5428492	27-Jun-1995	CURRENT DRIVER HAVING VOLTAGE TRANSITION FAILURE-BASED SHORT CIRCUIT PROTECTION CIRCUIT
SE-902		Granted	07/984187	20-Nov-1992	5416351	16-May-1995	ELECTROSTATIC DISCHARGE PROTECTION
28-MT-0047		Granted	08/001752	07-Jan-1993	5382825	17-Jan-1995	SPIRAL EDGE PASSIVATION STRUCTURE FOR SEMICONDUCTOR DEVICES
SE-915	A	Granted	08/440707	15-May-1995	5717617	10-Feb-1998	RATE CHANGE FILTER AND METHOD
SE-911		Granted	08/029860	25-Mar-1993	5272104	21-Dec-1993	BONDED WAFER PROCESS INCORPORATING DIAMOND INSULATOR
SE-911	A	Granted	08/513950	04-Dec-1995	5650639	22-Jul-1997	BONDED WAFER PROCESS INCORPORATING DIAMOND INSULATOR
SE-879/886		Granted	07/930930	14-Aug-1992	5440506	08-Aug-1995	SEMICONDUCTOR ROM DEVICE AND METHOD
SE-879/886	A	Granted	08/346178	21-Nov-1994	5586072	17-Dec-1996	SEMICONDUCTOR ROM DEVICE AND METHOD
SE-879/886	B	Granted	08/345689	21-Nov-1994	5563834	08-Oct-1996	SEMICONDUCTOR ROM DEVICE AND METHOD

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Client Ref	SubCase	Status	Appl #	Fil Date	Pat #	Iss Date	Title
SE-879/886	C	Granted	08/450878	26-May-1995	5650971	22-Jul-1997	SEMICONDUCTOR ROM DEVICE AND METHOD
SE-879/886	D	Granted	08/450879	26-May-1995	5544095	06-Aug-1996	SEMICONDUCTOR ROM DEVICE AND METHOD
28-SV-0080		Granted	07/980570	20-Nov-1992	5287071	15-Feb-1994	AMPLIFIER WITH HIGH COMMON MODE REJECTION
28-SV-0081		Granted	07/979209	20-Nov-1992	5406223	11-Apr-1995	AMPLIFIER SYSTEM FOR LOW LEVEL SIGNAL
SE-889		Granted	07/995442	23-Dec-1992	5312262	17-May-1994	DECOUPLING TOOL MECHANISM FOR ELECTRICAL CONNECTORS
SE-866/867		Granted	07/930170	14-Aug-1992	5493581	20-Feb-1996	DIGITAL DOWN CONVERTER AND METHOD
SE-866/867	A	Granted	08/478683	07-Jun-1995	5633815	27-May-1997	DIGITAL DOWN CONVERTER AND METHOD
SE-866/867	B	Granted	08/457234	01-Jun-1995	5617344	01-Apr-1997	DIGITAL DOWN CONVERTER AND METHOD
SE-866/867	C	Granted	08/456859	01-Jun-1995	5570392	29-Oct-1996	DIGITAL DOWN CONVERTER AND METHOD
SE-866/867	D	Granted	08/478682	07-Jun-1995	5757794	26-May-1998	DIGITAL DOWN CONVERTER AND METHOD
SE-933		Granted	08/023117	26-Feb-1993	5357089	18-Oct-1994	CIRCUIT AND METHOD FOR EXTENDING THE SAFE OPERATING AREA OF A BJT
28SV00076		Granted	08/082546	28-Jun-1993	5367211	22-Nov-1994	DIFFERENTIAL AMPLIFIER WITH HYSTERISIS
SE-932	A	Granted	08/471759	06-Jun-1995	5683939	04-Nov-1997	DIAMOND INSULATOR DEVICES AND METHOD OF FABRICATION
28SV0087		Granted	08/066854	25-May-1993	5359236	25-Oct-1994	INTEGRATED CIRCUIT THERMAL SENSOR

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Client Ref	Subcase	Status	Appl	Filing Date	Pat	Issue Date	Title
SE-901		Granted	08/030980	12-Mar-1993	5370568	06-Dec-1994	CURING OF A TUNGSTEN FILAMENT IN AN ION IMPLANTER
SE-926		Granted	08/066355	21-May-1993	5639688	17-Jun-1997	METHOD OF MAKING INTEGRATED CIRCUIT STRUCTURE WITH NARROW LINE WIDTHS
SE-926	A	Granted	08/460993	05-Jun-1995	5773891	30-Jun-1998	METHOD OF MAKING INTEGRATED CIRCUIT STRUCTURE WITH NARROW LINE WIDTHS
SE-919		Granted	08/053244	28-Apr-1993	5373183	13-Dec-1994	INTEGRATED CIRCUIT WITH IMPROVED REVERSE BIAS BREAKDOWN
SE-920		Granted	08/053243	28-Apr-1993	6008512	28-Dec-1999	SEMICONDUCTOR DEVICE WITH INCREASED MAXIMUM TERMINAL VOLTAGE
SE-920	A	Granted	08/463560	05-Jun-1995	5665634	09-Sep-1997	SEMICONDUCTOR DEVICE WITH INCREASED MAXIMUM TERMINAL VOLTAGE
SE-931		Granted	08/090978	09-Jul-1993	5341009	23-Aug-1994	FAST CHARGING MOS CAPACITOR STRUCTURE FOR HIGH MAGNITUDE VOLTAGE OF EITHER POSITIVE OR NEGATIVE POLARITY
SE-934		Granted	08/135093	12-Oct-1993	5561607	01-Oct-1996	METHOD OF MANUFACTURE OF MULTI-CELL INTEGRATED CIRCUIT ARCHITECTURE
SE-948		Granted	08/106251	13-Aug-1993	5581475	03-Dec-1996	METHOD FOR INTERACTIVELY TAILORING TOPOGRAPHY OF INTEGRATED CIRCUIT LAYOUT IN ACCORDANCE WITH ELECTROMIGRATION MODEL-BASED MINIMUM WIDTH METAL AND
SE-909	A	Granted	08/292588	18-Aug-1994	5448102	05-Sep-1995	TRENCH ISOLATION STRESS RELIEF
SE-909	B	Granted	08/465246	05-Jun-1995	5683075	04-Nov-1997	TRENCH ISOLATION STRESS RELIEF
SE-916		Granted	08/125411	22-Sep-1993	5552345	03-Sep-1996	DIE SEPARATION METHOD FOR SILICON ON DIAMOND CIRCUIT STRUCTURES
SE-929		Granted	08/108358	18-Aug-1993	5585661	17-Dec-1996	SUBMICRON BONDED SOI BY TRENCH PLANARIZATION
RD 15503		Granted	07/595800	02-Apr-1984	4871617	03-Oct-1989	OHMIC CONTACTS AND INTERCONNECTS TO SILICON AND METHOD OF MAKING SAME

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	FilDate	Pat	IssDate	Title
SE-938		Granted	08/123157	07-Sep-1993	5395774	07-Mar-1995	METHODS FOR FORMING A TRANSISTOR HAVING AN EMITTER WITH ENHANCED EFFICIENCY
SE-952		Granted	08/118063	08-Sep-1993	5516625	14-May-1996	FILL & ETCHBACK PROCESS USING DUAL PHOTORESIST SACRIFICIAL LAYER & TWO-STEP ETCHING PROCESS FOR PLANARIZING OXIDE-FILLED SHALLOW TRENCH STRUCTURE
SE-950		Granted	08/271292	06-Jul-1994	5450326	12-Sep-1995	GRAPHICAL DISPLAY DISCRIMINANT FACTOR INDICATOR FOR ANOMALY IDENTIFICATION IN SEMICONDUCTOR MANUFACTURE BATCH PROCESS
SE-906		Granted	07/939786	03-Sep-1992	5387555	07-Feb-1995	BONDED WAFER PROCESSING WITH METAL SILICIDATION
SE-906	A	Granted	08/351933	08-Dec-1994	5569620	29-Oct-1996	BONDED WAFER PROCESSING WITH METAL SILICIDATION
SE-954-SP		Granted	08/090617	12-Jul-1993	5809410	15-Sep-1998	LOW VOLTAGE RF AMPLIFIER AND MIXER WITH SINGLE BIAS BLOCK AND METHOD
SE-957		Granted	08/135092	12-Oct-1993	5576695	19-Nov-1996	RESISTANCE-MEASUREMENT BASED ARRANGEMENT FOR MONITORING INTEGRITY OF TRAVEL PATH GROUND LINK IN ELECTRONIC COMPONENT HANDLING APPARATUS
SE-959		Granted	08/314489	28-Sep-1994	5637908	10-Jun-1997	STRUCTURE AND TECHNIQUE FOR TAILORING EFFECTIVE RESISTIVITY OF A SIPOS LAYER BY PATTERNING AND CONTROL OF DOPANT INTRODUCTION
SE-922		Granted	07/993585	21-Dec-1992	5345236	06-Sep-1994	ANALOG-TO-DIGITAL CONVERTER AND METHOD
SE-953		Granted	08/198002	17-Feb-1994	5574618	12-Nov-1996	ESD PROTECTION USING SCR CLAMPING
28-SV-0085		Granted	08/192398	03-Feb-1994	5583442	10-Dec-1996	DIFFERENTIAL VOLTAGE MONITOR USING A BRIDGE CIRCUIT WITH RESISTORS ON AND OFF OF AN INTEGRATED CIRCUIT
SE-956		Granted	08/190998	03-Feb-1994	5526768	18-Jun-1996	METHOD FOR PROVIDING A SILICON AND DIAMOND SUBSTRATE HAVING A CARBON TO SILICON TRANSITION LAYER AND APPARATUS THEREOF
SE-956	A	Granted	08/587953	17-Jan-1996	5782975	21-Jul-1998	METHOD FOR PROVIDING A SILICON AND DIAMOND SUBSTRATE HAVING A CARBON TO SILICON TRANSITION LAYER AND APPARATUS THEREOF
SE-963		Granted	08/180666	13-Jan-1994	5446368	29-Aug-1995	VOLTAGE INDEPENDENT SYMMETRICAL CURRENT SOURCE WITH CROSS-COUPLED TRANSISTORS

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Cred Ref	SubCase	Status	Appl	FilDate	Patt	IssDate	Title
28-SV-0093		Granted	08/204710	02-Mar-1994	5508551	16-Apr-1996	CURRENT MIRROR WITH SATURATION LIMITING
28-SV-0092		Granted	08/204718	02-Mar-1994	5608259	04-Mar-1997	REVERSE CURRENT FLOW PREVENTION IN A DIFFUSED RESISTOR
28-SV-0090		Granted	08/204711	02-Mar-1994	5420499	30-May-1995	CURRENT RISE AND FALL TIME LIMITED VOLTAGE FOLLOWER
SE-974		Granted	08/497124	30-Jun-1995	5546038	13-Aug-1996	SCR-INDUCTOR TRANSIENT CLAMP
SE-973		Pending	08/276290	18-Jul-1994			CMOS INTEGRATED CIRCUIT ARCHITECTURE INCORPORATION DEEP IMPLANTED EMITTER REGION TO FORM AUXILIARY BIPOLAR TRANSISTOR
SE-935/936		Granted	08/299741	01-Sep-1994	5541538	30-Jul-1996	HIGH SPEED COMPARATOR
SE-981		Granted	08/235979	02-May-1994	5519732	21-May-1996	DIGITAL BASEBAND TO IF CONVERSION IN CELLULAR BASE STATIONS
28-SV-0091	A	Granted	08/562609	24-Nov-1995	5610792	11-Mar-1997	APPARATUS FOR CONTROLLING THE RESET OF A BUS CONNECTED TRANSCEIVER
SE-976		Granted	08/265355	24-Jun-1994	5423889	13-Jun-1995	PROCESS FOR MANUFACTURING A MULTI-PORT ADHESIVE DISPENSING TOOL
SE-982		Granted	08/279027	22-Jul-1994	5622890	22-Apr-1997	METHOD OF MAKING CONTACT REGIONS FOR NARROW TRENCHES IN SEMICONDUCTOR DEVICES
SE-983		Granted	08/301622	07-Sep-1994	5574572	12-Nov-1996	VIDEO SCALING METHOD AND DEVICE
SE-984/985		Granted	08/269470	30-Jun-1994	5808489	15-Sep-1998	HIGH SPEED A/D CONVERTER AND SLEW CONTROLLED PULSE DETECTOR
SE-987		Granted	08/497008	30-Jun-1995	5621478	15-Apr-1997	MULTISTANDARD DECODER FOR VIDEO SIGNALS AND VIDEO SIGNAL DECODING METHOD
SE-988		Granted	08/497181	30-Jun-1995	5619270	08-Apr-1997	SAMPLE RATE CONVERTER AND SAMPLE RATE CONVERSION METHOD

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Client Ref	SubCase	St Status	Appl	F Date	Patt	Iss Date	Title
SE-989		Granted	08/496868	30-Jun-1995	5621477	15-Apr-1997	DIGITAL DECODER AND METHOD FOR DECODING COMPOSITE VIDEO SIGNALS
SE-993		Granted	08/267436	29-Jun-1994	5515417	07-May-1996	GROUND KEY DETECTOR FOR A SLIC
SE-994		Granted	08/266567	28-Jun-1994	5614867	25-Mar-1997	CURRENT FOLLOWER WITH ZERO INPUT IMPEDANCE
SE-1001-TL		Granted	08/380410	30-Jan-1995	5528682	18-Jun-1996	DOUBLE DUTY CAPACITOR CIRCUIT AND METHOD
28-MT-0066		Granted	08/332300	31-Oct-1994	5569957	29-Oct-1996	LOW INDUCTANCE POWER PACKAGE DESIGN
SE-991		Granted	08/267434	29-Jun-1994	5515434	07-May-1996	IMPEDANCE SETTING CIRCUIT FOR A SLIC
SE-972	A	Granted	08/543754	16-Oct-1995	5652153	29-Jul-1997	JFET STRUCTURES FOR SEMICONDUCTOR DEVICES WITH COMPLEMENTARY BIPOLAR TRANSISTORS & METHOD
SE-995		Granted	08/269133	30-Jun-1994	5517565	14-May-1996	AN INTEGRATED RINGER RELAY CIRCUIT AND METHOD
SE-971		Granted	08/419610	10-Apr-1995	5644309	01-Jul-1997	DIGITAL COMPONENT TESTING APPARATUS AND METHOD
SE-1022-MS		Granted	08/537051	29-Sep-1995	5621355	15-Apr-1997	SAMPLED DATA BIASING OF CONTINUOUS TIME INTEGRATED CIRCUIT
SE-1010-TD		Granted	08/405660	17-Mar-1995	5614422	25-Mar-1997	PROCESS FOR DOPING TWO LEVELS OF A DOUBLE POLY BIPOLAR TRANSISTOR AFTER FORMATION OF SECOND POLY LAYER
SE-1020-TL		Granted	08/340342	14-Nov-1994	5649009	15-Jul-1997	A DIFFERENTIAL LONGITUDINAL AMPLIFIER FOR SUBSCRIBER LINE INTERFACE CIRCUIT
SE-1025-TD		Granted	08/503048	17-Jul-1995	5650344	22-Jul-1997	NON-UNIFORMLY NITRIDED GATE OXIDE AND METHOD
SE-1027-TD		Granted	08/387233	13-Feb-1995	5547896	20-Aug-1996	DIRECT ETCH FOR THIN FILM RESISTOR USING A HARD MASK

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Ap Status	Apl #	FilDate	Pat #	IssDate	Title
SE-1041-TD		Granted	08/383261	03-Feb-1995	5567978	22-Oct-1996	HIGH VOLTAGE, JUNCTION ISOLATION SEMICONDUCTOR DEVICE HAVING DUAL CONDUCTIVITY TYPE BURIED REGIONS AND ITS PROCESS OF MANUFACTURE
SE-1023-SP		Granted	08/331015	28-Oct-1994	5598157	28-Jan-1997	SIGMA DELTA ANALOG TO DIGITAL CONVERTER WITH THREE POINT CALIBRATION APARATUS AND METHOD
SE-1030-SP		Granted	08/441726	16-May-1995	5576654	19-Nov-1996	A BI-MOS DRIVER CIRCUIT WITH REDUCED POWER SUPPLY GLITCHES
SE-1039-SP		Granted	08/372118	13-Jan-1995	5636274	03-Jun-1997	SWITCH CONTROLLER AND METHOD
SE-1057-TL		Granted	08/380413	30-Jan-1995	5812658	22-Sep-1998	METHOD AND CIRCUIT FOR FAILSAFE SWITCH-HOOK DETECTION DURING FAULT IN A TELEPHONE SYSTEM
SE-1058-TL		Granted	08/380411	30-Jan-1995	5659570	19-Aug-1997	CIRCUIT AND METHOD FOR LOOPBACK TEST AND ON-HOOK TRANSMISSION INTEGRATED INTO A TELEPHONE SUBSCRIBER LINE INTERFACE CIRCUIT
SE-1050-MS		Granted	08/505671	21-Jul-1995	5621307	15-Apr-1997	FAST RECOVERY TEMPERATURE COMPENSATED PRECISION REFERENCE SOURCE
SE-1036-TD		Granted	08/705536	29-Aug-1996	5798557	25-Aug-1998	LID WAFER BOND PACKAGING AND MICROMACHINING
SE-1048-TD		Granted	08/443242	17-May-1995	5603779	18-Feb-1997	BONDED WAFER
SE-1069-AP		Granted	08/395814	28-Feb-1995	5724370	03-Mar-1998	CRC GENERATION & DETECTION METHOD
SE-1070-AP		Granted	08/395590	28-Feb-1995	5526392	11-Jun-1996	METHOD OF SCALING THE OUTPUTS OF A BINARY COUNTER
SE-1071-AP		Granted	08/395863	28-Feb-1995	5678030	14-Oct-1997	MODIFICATION OF TIMING IN AN EMULATOR CIRCUIT AND METHOD
SE-1072-AP		Granted	08/395591	28-Feb-1995	5661736	26-Aug-1997	MULTIPLE USE TIMER AND METHOD FOR PULSE WIDTH GENERATION, ECHO FAILURE DETECTION, AND RECEIVE PULSE WIDTH MEASUREMENT
SE-1034-TD		Granted	08/382346	01-Feb-1995	5625566	29-Apr-1997	CONFIGURATION DEPENDENT AUTO-BIASING OF BIPOLAR TRANSISTOR

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	FiDate	Patent	IssDate	Title
SE-939		Granted	08/552711	03-Nov-1995	5669599	22-Sep-1997	MAGNETIC BOATS
SE-1000-TD		Granted	08/386785	10-Feb-1995	5682336	28-Oct-1997	SIMULATION OF NOISE BEHAVIOR OF NON-LINEAR CIRCUIT
SE-1087-SP		Granted	08/438251	10-May-1995	5617090	01-Apr-1997	MULTICHANNEL SIGMA-DELTA A/D CONVERTERS WITH IMPROVED THROUGHPUT
SE-1081-IP		Granted	08/438636	10-May-1995	5610503	11-Mar-1997	LOW VOLTAGE DC-TO-DC POWER CONVERTER INTEGRATED CIRCUIT AND RELATED METHODS
SE-1074-MS		Granted	08/490566	15-Jun-1995	5525869	11-Jun-1996	EFFICIENT BATTERY OPERATED INVERTER CIRCUIT FOR CAPACITIVE LOADS SUCH AS ELECTROLUMINESCENT LAMPS
SE-1075-MS		Granted	08/490016	13-Jun-1995	5557175	17-Sep-1996	BATTERY OPERATED INVEERTER CIRCUIT FOR CAPACITIVE LOADS SUCH AS ELECTROLUMINESCENT LAMPS
SE-1097-AP		Granted	08/505695	21-Jul-1995	5642247	24-Jun-1997	AUTOMATIC FAULT MONITORING SYSTEM AND MOTOR CONTROL SYSTEM INCORPORATING SAME
SE-1104-TD		Granted	08/481115	07-Jun-1995	5750432	12-May-1998	DEFECT CONTROL IN FORMATION OF DIELECTRICALLY ISOLATED SEMICONDUCTOR DEVICE REGIONS
SE-1107-TD		Granted	08/497404	30-Jun-1995	5773151	30-Jun-1998	SEMI-INSULATING WAFER
SE-1102-MS		Granted	08/490952	15-Jun-1995	5539707	23-Jul-1996	ELECTROLUMINESCENT LAMP DRIVER SYSTEM
SE-1131-TD		Granted	08/461951	05-Jun-1995	5646067	08-Jul-1997	METHOD OF BONDING WAFERS HAVING VIAS INCLUDING CONDUCTIVE MATERIAL
SE-1132-TD		Granted	08/461643	05-Jun-1995	5608264	04-Mar-1997	SURFACE MOUNTABLE INTEGRATED CIRCUIT WITH CONDUCTIVE VIAS
SE-1133-TD		Granted	08/461037	05-Jun-1995	5814889	29-Sep-1998	INTEGRATED CIRCUIT WITH COAXIAL ISOLATION AND METHOD
SE-1134-TD		Granted	08/463388	05-Jun-1995	5668409	16-Sep-1997	INTEGRATED CIRCUIT WITH EDGE CONNECTIONS AND METHOD

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Ap...	...Date	Pat...	IssDate	Title
SE-1135-TD		Granted	08/462876	05-Jun-1995	5682062	28-Oct-1997	SYSTEM FOR INTERCONNECTING STACKED INTEGRATED CIRCUITS
SE-1114-TD		Granted	08/512323	08-Aug-1995	5696452	09-Dec-1997	ARRANGEMENT & METHOD FOR IMPROVING ROOM-TEMPERATURE TESTABILITY OF CMOS INTEGRATED CIRCUITS OPTIMIZED FOR CRYOGENIC TEMPERATURE OPERATOR
SE-1052-TD		Granted	08/474559	07-Jun-1995	5777362	07-Jul-1998	HIGH EFFICIENCY QUASI-VERTICAL DMOS IN A CMOS OR BICMOS PROCESS
SE-1053-TD		Granted	08/483691	07-Jun-1995	5689129	18-Nov-1997	HIGH EFFICIENCY POWER MOS SWITCH
SE-1054-TD		Granted	08/483692	07-Jun-1995	5684305	04-Nov-1997	PILOT TRANSISTOR FOR QUASI-VERTICAL DMOS
SE-1122-TL		Granted	08/494395	26-Jun-1995	5736885	07-Apr-1998	OFFSET ADJUSTMENT FOR FULLY DIFFERENTIAL AMPLIFIERS
SE-1123-TL		Granted	08/493454	23-Jun-1995	5617473	01-Apr-1997	SIGN BIT INTEGRATOR AND METHOD
SE-1062-SP		Granted	08/515435	15-Aug-1995	5701097	23-Dec-1997	STATISTICALLY BASED CURRENT GENERATOR CIRCUIT
SE-1060-TD		Granted	08/481116	07-Jun-1995	5580816	03-Dec-1996	LOCAL OXIDATION PROCESS FOR HIGH FIELD THRESHOLD APPLICATIONS
SE-1028-LN		Granted	08/507192	26-Jul-1995	5581444	03-Dec-1996	DEVICE AND METHOD FOR ENHANCING THERMAL AND HIGH FREQUENCY PERFORMANCE OF INTEGRATED CIRCUIT PACKAGES
SE-1147-TL		Granted	08/509462	31-Jul-1995	5712870	27-Jan-1998	PACKET HEADER GENERATION AND DETECTION CIRCUITRY
SE-1151-TL		Granted	08/509589	31-Jul-1995	5675339	07-Oct-1997	A/D REFERENCE LEVEL ADJUSTMENT CIRCUIT TO MAINTAIN OPTIMUM DYNAMIC RANGE AT THE A/D
SE-1148-TL		Granted	08/509588	31-Jul-1995	5654991	05-Aug-1997	FAST ACQUISITION BIT TIMING LOOP CIRCUIT METHOD AND APPARATUS
SE-1149-TL		Granted	08/509587	31-Jul-1995	5883921	16-Mar-1999	SHORT BURST ACQUISITION CIRCUIT AND METHOD FOR DIRECT SEQUENCE SPREAD SPECTRUM LINKS

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	FilDate	Patt	IssDate	Title
SE-1150-TL		Granted	08/509586	31-Jul-1995	5732105	24-Mar-1998	A METHOD OF ESTIMATING SIGNAL QUALITY FOR A DIRECT SEQUENCE SPREAD SPECTRUM RECEIVER DEVICE
SE-1153-TL		Granted	08/512405	08-Aug-1995	5606288	25-Feb-1997	DIFFERENTIAL TRANSIMPEDANCE AMPLIFIER
SE-1117-TL		Granted	08/527548	13-Sep-1995	5610093	11-Mar-1997	METHOD OF MANUFACTURING A PROGRAMMABLE HYBRID BALANCE NETWORK
SE-1037-TD		Granted	08/536257	29-Sep-1995	5830279	03-Nov-1998	DEVICE AND METHOD FOR IMPROVING CORROSION RESISTANCE AND ETCH TOOL INTEGRITY IN DRY METAL ETCHING
SE-1106-TD		Granted	08/596079	06-Feb-1996	5883414	16-Mar-1999	ELECTROSTATIC DISCHARGE PROTECTION DEVICE
SE-1138-TL		Granted	08/506978	28-Jul-1995	5654662	05-Aug-1997	INVERTED BJT CURRENT SOURCES/SINKS IN RF CIRCUITS AND METHODS
SE-1162-IP		Granted	08/602287	16-Feb-1996	5717322	10-Feb-1998	METHOD TO IMPROVE THE PEAK-CURRENT LIMIT IN SLOPE-COMPENSATED, CURRENT-MODE DC/DC CONVERTERS
SE-1158-IP		Granted	08/799959	14-Feb-1997	5793193	11-Aug-1998	DC-TO-DC CONVERTER HAVING ENHANCED CONTROL FEATURES AND ASSOCIATED METHODS
SE-1175-MS		Granted	08/584366	11-Jan-1996	5668468	16-Sep-1997	COMMON MODE STABILIZING CIRCUIT AND METHOD
SE-1118-TL		Granted	08/552379	03-Nov-1995	5717736	10-Feb-1998	TESTING CIRCUIT FOR A CODEC HYBRID BALANCE NETWORK
SE-1137-AP		Granted	08/512417	08-Aug-1995	5614852	25-Mar-1997	WIDE COMMON MODE RANGE COMPARATOR AND METHOD
SE-999		Granted	08/427231	24-Apr-1995	5602052	11-Feb-1997	METHOD OF FORMING DUMMY ISLAND CAPACITOR
SE-1155-TL		Granted	08/608728	29-Feb-1996	5831423	03-Nov-1998	PHASE METER AND METHOD OF PROVIDING A VOLTAGE INDICATIVE OF A PHASE DIFFERENCE
SE-1179-MS		Granted	08/601401	14-Feb-1996	5798724	29-Aug-1998	INTERPOLATING DIGITAL TO ANALOG CONVERTER ARCHITECTURE FOR IMPROVED SPURIOUS SIGNAL SUPPRESSION

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	Subcase	Status	Appl	FilDate	Pat	IssDate	Title
SE-1119-TL		Granted	08/590940	24-Jan-1996	5680072	21-Oct-1997	DIFFERENTIAL INTERPOLATION SWITCHED CAPACITOR FILTER AND METHOD
SE-1173-TD		Granted	08/586556	16-Jan-1996	5670413	23-Sep-1997	METHOD & APPARATUS FOR RADIATION HARDENED ISOLATION
SE-1191-MS		Granted	08/613381	07-Mar-1996	5677599	14-Oct-1997	A CIRCUIT FOR DRIVING AN ELECTROLUMINESCENT LAMP
SE-1178-MS		Granted	08/608812	29-Feb-1996	5742204	21-Apr-1998	DIGITALLY PROGRAMMABLE DIFFERENTIAL ATTENUATOR WITH TRACKING COMMON MODE REFERENCE
SE-1061-MS		Granted	08/560289	17-Nov-1995	5666083	09-Sep-1997	IMPROVED DISCRETE PROGRAMMING METHODOLOY AND CIRCUIT FOR AN ACTIVE TRANSCONDUCTANCE C-FILTER
SE-1164-TD		Granted	08/637132	24-Apr-1996	5717243	10-Feb-1998	AN INTEGRATED CIRCUIT WITH AN IMPROVED INDUCTOR STRUCTURE AND METHOD OF FABRICATION
SE-1089-AP	A	Granted	08/652933	24-May-1996	5675281	07-Oct-1997	METHOD AND CIRCUIT FOR PREVENTING FORWARD BIAS OF A PARASITIC DIODE IN AN INTEGRATED CIRCUIT
SE-905-TD	A	Granted	08/573099	15-Dec-1995	5729038	17-Mar-1998	SILICON GLASS-BONDED WAFERS
SE-822-SP	E	Granted	08/645139	13-May-1996	5659261	19-Aug-1997	ANALOG-TO-DIGITAL CONVERTER AND METHOD OF FABRICATION
SE-873	C	Granted	08/612695	08-Mar-1996	5650658	22-Jul-1997	INTEGRATION OF HIGH VOLTAGE LATERAL CMOS DEVICES IN LOW VOLTAGE MOS ARCHITECTURE USING CMOS COMPATIBLE PROCESS STEPS
SE-822-SP	D	Granted	08/630874	02-Apr-1996	5682111	28-Oct-1997	ANALOG-TO-DIGITAL CONVERTER AND METHOD OF FABRICATION
SE-1196-TD		Granted	08/646471	08-May-1996	5856700	05-Jan-1999	SEMICONDUCTOR DEVICE WITH DOPED SEMICONDUCTOR AND DIELECTRIC TRENCH SIDEWALL LAYERS
SE-1188-TD		Granted	08/643295	08-May-1996	5837603	17-Nov-1998	PLANARIZATION METHOD BY THE USE OF PARTICLE DISPERSION AND SUBSEQUENT THERMAL FLOW
SE-1112-LN		Granted	08/640108	30-Apr-1996	5686822	11-Nov-1997	METHOD OF MAKING A REFERENCE CURRENT GENERATOR

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Cy Status	Appl. #	Appl. Date	Pat. #	Iss. Date	Title
SE-1078-TD		Granted	08/650688	20-May-1996	5825092	20-Oct-1998	INTEGRATED CIRCUIT WITH AN AIR BRIDGE HAVING A LID
SE-1099-TD		Granted	08/587692	17-Jan-1996	5587103	24-Dec-1996	COMPOSITION, AND METHOD FOR USING SAME, FOR ETCHING METALLIC ALLOYS FROM A SUBSTRATE
SE-1063-TD		Granted	08/654316	28-May-1996	5965933	12-Oct-1999	SEMICONDUCTOR PACKAGING APPARATUS
SE-1033-TD		Granted	08/650762	20-May-1996	5949144	07-Sep-1999	PRE-BOND CAVITY AIR BRIDGE
SE-1211-TD		Granted	08/637937	26-Apr-1996	5933746	03-Aug-1999	WAFER TRENCH ARTICLE AND PROCESS
SE-1198-TD		Granted	08/654393	28-May-1996	5804846	08-Sep-1998	PROCESS FOR FORMING A SELF-ALIGNED RAISED SOURCE/DRAIN MOS DEVICE AND DEVICE THEREFROM
SE-1038-IP		Granted	08/493824	22-Jun-1995	5627489	06-May-1997	LEVEL SHIFTER WITH IMPROVED REJECTION OF VOLTAGE VARIATIONS
SE-1157-SP		Granted	08/671025	25-Jun-1996	5930301	27-Jul-1999	UP-CONVERSION MECHANISM EMPLOYING SIDE LOBE-SELECTIVE PRE-DISTORTION FILTER AND FREQUENCY REPLICA-SELECTING BANDPASS FILTER RESPECTIVELY INSTALLED UPSTREAM
SE-1182-TD		Granted	08/669066	24-Jun-1996	5920219	06-Jul-1999	CLOCK -CONTROLLED PRECISION MONOSTABLE CIRCUIT
SE-811	A	Pending	08/674585	02-Jul-1996			NEGATIVE BIASING OF ISOLATION TRENCH FILL TO ATTRACT MOBILE POSITIVE IONS AWAY FROM BIPOLAR DEVICE REGIONS
SE-1250-TD		Granted	08/666258	20-Jun-1996	5808353	15-Sep-1998	RADIATION HARDENED DIELECTRIC FOR EEPROM
SE-1041-TD	A	Granted	08/683599	15-Jul-1996	5837553	17-Nov-1998	HIGH VOLTAGE, JUNCTION ISOLATION SEMICONDUCTOR DEVICE HAVING DUAL CONDUCTIVITY TYPE BURIED REGIONS AND ITS PROCESS OF MANUFACTURE
SE-1176-MS		Granted	08/606958	23-Feb-1996	5953379	14-Sep-1999	CURRENT-CONTROLLED CARRIER TRACKING FILTER FOR IMPROVED SPURIOUS SIGNAL SUPPRESSION
SE-1177-MS		Granted	08/637140	24-Apr-1996	5736903	07-Apr-1998	CARRIER BUFFER HAVING CURRENT-CONTROLLED TRACKING FILTER FOR SPURIOUS SIGNAL SUPPRESSION

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	FilDate	Pat	IssDate	Title
SE-1218-TD		Granted	08/671243	27-Jun-1996	5841169	24-Nov-1998	INTEGRATED CIRCUIT CONTAINING DEVICES DIELECTRICALLY ISOLATED AND JUNCTION ISOLATED FROM A SUBSTRATE
SE-1219-TD		Granted	08/671157	28-Jun-1996	5817564	06-Oct-1998	DOUBLE DIFFUSED MOS DEVICE AND METHOD
SE-1228-TD		Granted	08/673396	28-Jun-1996	5663860	02-Mar-1998	HIGH VOLTAGE PROTECTION CIRCUITS
28-SP-1401	A	Granted	08/656987	06-Jun-1996	5870266	09-Feb-1999	BRIDGE CONTROL CIRCUIT AND METHOD
SE-1186-MS		Granted	08/671781	20-Jun-1996	5841324	24-Nov-1998	CHARGE BASED FREQUENCY LOCKED LOOP AND METHOD
SE-1137-AP	A	Granted	08/719873	25-Sep-1996	5789949	04-Aug-1998	WIDE COMMON MODE RANGE COMPARATOR AND METHOD
SE-1248-TD		Granted	08/707271	03-Sep-1996	5770880	23-Jun-1998	P COLLECTOR HV PMOS SWITCH VT ADJUSTED SOURCE
SE-1235-DA		Granted	08/714019	11-Sep-1996	5790060	04-Aug-1998	DIGITAL-TO-ANALOG CONVERTER HAVING ENHANCED CURRENT STEERING AND ASSOCIATED METHOD
SE-1215-DA		Granted	08/712027	11-Sep-1996	5771012	23-Jun-1998	INTEGRATED CIRCUIT ANALOG-TO-DIGITAL CONVERTER AND ASSOCIATED CALIBRATION METHOD AND APPARATUS
SE-1092-TL		Granted	08/687995	29-Jul-1996	5767757	16-Jun-1998	ELECTRICALLY VARIABLE R/C NETWORK AND METHOD
SE-1009-DA		Granted	08/707380	04-Sep-1996	5923209	13-Jul-1999	TWO TRIM CURRENT SOURCE AND METHOD FOR A DIGITAL-TO-ANALOG CONVERTER
SE-1083-TD		Granted	08/726183	04-Oct-1996	5708549	13-Jan-1998	INTEGRATED CIRCUIT HAVING ENHANCED TRANSIENT VOLTAGE PROTECTION AND ASSOCIATED METHODS
SE-1048-TD	A	Granted	08/710694	19-Sep-1996	5744852	28-Apr-1998	BONDED WAFER
SE-822-SP	F	Granted	08/739898	30-Oct-1996	5994755	30-Nov-1999	ANALOG-TO-DIGITAL CONVERTER AND METHOD OF FABRICATION

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Client Ref	SubCase	Status	Appl	FilDate	Pat	IssDate	Title
SE-1032-TD		Granted	08/726659	07-Oct-1996	5807783	15-Sep-1998	SURFACE MOUNT DIE BY HANDLE REPLACEMENT
SE-1254-AP		Granted	08/738393	24-Oct-1996	5719326	17-Feb-1998	RECONFIGURABLE FILTER SYSTEM
SE-921-TD	B	Granted	08/733368	17-Oct-1996	5872044	16-Feb-1999	LATE PROCESS METHOD AND APPARATUS FOR TRENCH ISOLATION
SE-1026-TD	A	Granted	08/754596	20-Nov-1996	5833758	10-Nov-1998	PLASMA CLEANING METHOD FOR IMPROVED DIE TO SUBSTRATE SOLDERABILITY
SE-992	A	Granted	08/741639	28-Oct-1996	5841182	24-Nov-1998	CAPACITOR STRUCTURE IN A BONDED WAFER AND METHOD OF FABRICATION
SE-1234-TL		Granted	08/725924	04-Oct-1996	5812029	22-Sep-1998	GAIN CONTROL CIRCUIT AND METHOD
SE-921-TD	C	Granted	08/745104	07-Nov-1996	5920108	06-Jul-1999	LATE PROCESS METHOD AND APPARATUS FOR TRENCH ISOLATION
SE-967	B	Granted	08/754597	20-Nov-1996	5882423	16-Mar-1999	PLASMA CLEANING METHOD FOR IMPROVED INK BRAND PERMANENCY ON IC PACKAGES WITH METALLIC PARTS
SE-1265-WR		Granted	08/781736	10-Jan-1997	5949695	07-Sep-1999	INTERPOLATOR USING A PLURALITY OF POLYNOMIAL EQUATIONS AND ASSOCIATED METHODS
SE-1266-WR		Granted	08/781334	10-Jan-1997	5764113	09-Jun-1998	RE-SAMPLING CIRCUIT AND ASSOCIATED METHOD
SE-758	C	Granted	08/786569	21-Jan-1997	5892264	06-Apr-1999	HIGH FREQUENCY ANALOG TRANSISTORS, METHOD OF FABRICATION AND CIRCUIT IMPLEMENTATION
SE-1010-TD	A	Granted	08/775360	03-Jan-1997	5776814	07-Jul-1998	PROCESS FOR DOPING TWO LEVELS OF A DOUBLE POLY BIPOLAR TRANSISTOR AFTER FORMATION OF SECOND POLY LAYER
SE-1010-TD	B	Granted	08/775361	03-Jan-1997	5686322	11-Nov-1997	PROCESS FOR DOPING TWO LEVELS OF A DOUBLE POLY BIPOLAR TRANSISTOR AFTER FORMATION OF SECOND POLY LAYER
SE-1245-TD		Granted	08/771944	23-Dec-1996	5914280	22-Jun-1999	DEEP TRENCH ETCH ON BONDED SILICON WAFER

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Reference	Sub Case	Status	Appl.	Fil Date	Pat.	Iss Date	Title
SE-1261-TD		Granted	08/798039	06-Feb-1997	5830048	03-Nov-1998	PIVOT SAMPLE BLOCK CROSS-SECTION TOOL
SE-1094-LN	A	Granted	08/777101	30-Dec-1996	5923207	13-Jul-1999	COMPLEMENTARY MULTIPLEXER WITH LOW DISABLED-OUTPUT CAPACITANCE, AND METHOD
SE-812	D	Granted	08/783792	15-Jan-1997	5780311	14-Jul-1998	BONDED WAFER PROCESSING
SE-1517-PD		Granted	09/344868	28-Jun-1999	6242784	05-Jun-2001	EDGE TERMINATION FOR SILICON POWER DEVICES
SE-1468-TD		Pending	09/345261	30-Jun-1999			METHOD FOR MAKING A DIFFUSED BACK-SIDE LAYER ON A BONDED-WAFER WITH A THICK BOND OXIDE
SE-1467-TD		Pending	09/342948	29-Jun-1999			BRUSHLESS MULTIPASS SILICON WAFER CLEANING PROCESS FOR POST CHEMICAL MECHANICAL POLISHING USING IMMERSION
SE-1504-TD		Pending	09/343845	30-Jun-1999			METHOD OF MANUFACTURING A PLATED ELECTRONIC TERMINATION
SE-1497-TD		Pending	09/339274	23-Jun-1999			INTEGRATED RESISTIVE CONTACT
SE-1478-TD		Granted	09/358266	21-Jul-1999	6259151	10-Jul-2001	USE OF BARRIER REFRACTIVE OR ANTI-REFLECTIVE LAYER TO IMPROVED LASER TRIM CHARACTERISTICS OF THIN FILM RESISTORS
SE-1498-TL		Granted	09/365238	30-Jul-1999	6137189	24-Oct-2000	LINE CIRCUIT APPARATUS FOR SUPPLYING POWER TO A TELEPHONE SET IN TELECOMMUNICATION SYSTEMS
SE-1053-TD	B	Pending	09/392806	09-Sep-1999			HIGH EFFICIENCY POWER MOS SWITCH
SE-1278-TD		Granted	08/799793	12-Feb-1997	5976944	02-Nov-1999	INTEGRATED CIRCUIT WITH THIN FILM RESISTORS AND A METHOD FOR CO-PATTERNING THIN FILM RESISTORS WITH DIFFERENT COMPOSITONS
SE-1004-TD	A	Granted	08/810127	25-Feb-1997	5895953	20-Apr-1999	METHOD FOR MAKING OHMIC CONTACT TO LIGHTLY DOPED ISLAND FROM A SILICIDE BURIED LAYER AND APPLICATION
SE-1301-WR		Granted	08/819846	17-Mar-1997	5982807	09-Nov-1999	HIGH DATA RATE SPREAD SPECTRUM TRANSCEIVER AND ASSOCIATED METHODS

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	ClaimsStat	Appl	FilDate	Patl	IssDate	Title
SE-982	A	Granted	08/845214	21-Apr-1997	5962908	05-Oct-1999	METHOD OF MAKING CONTACT REGIONS FOR NARROW TRENCHES IN SEMICONDUCTOR DEVICES
SE-1187-TD		Granted	08/855385	13-May-1997	5945699	31-Aug-1999	REDUCED WIDTH, DIFFERENTIALLY DOPED VERTICAL JFET DEVICE
SE-1274-AP		Granted	08/858845	19-May-1997	5900643	04-May-1999	INTEGRATED CIRCUIT CHIP STRUCTURE FOR IMPROVED PACKAGING
SE-765	C	Granted	08/868813	04-Jun-1997	5929502	27-Jul-1999	PUNCH THROUGH DIODES AND APPLICATIONS
SE-765	D	Granted	08/868815	04-Jun-1997	5929503	27-Jul-1999	PUNCH THROUGH DIODES AND APPLICATIONS
SE-1120-TL	A	Granted	08/873902	13-Jun-1997	5856742	05-Jan-1999	TEMPERATURE INSENSITIVE BANDGAP VOLTAGE GENERATOR TRACKING POWER SUPPLY VARIATIONS
SE-1159-IP		Granted	08/800420	14-Feb-1997	5821740	13-Oct-1998	DC-TO-DC CONVERTER HAVING FAST OVER-CURRENT DETECTION AND ASSOCIATED METHODS
SE-1276-DA		Granted	08/885273	30-Jun-1997	5861826	19-Jan-1999	METHOD AND APPARATUS FOR CALIBRATING INTEGRATED CIRCUIT ANALOG-TO-DIGITAL CONVERTERS
SE-954-SP	A	Granted	08/884635	27-Jun-1997	6018270	25-Jan-2000	LOW VOLTAGE RF AMPLIFIER AND MIXER WITH SINGLE BIAS BLOCK AND METHOD
SE-1264-TD		Granted	08/885897	30-Jun-1997	5892223	06-Apr-1999	MULTILAYER MICROTIP PROBE AND METHOD
SE-1304-DA		Granted	08/885274	30-Jun-1997	5892472	06-Apr-1999	PROCESSOR CONTROLLED ANALOG-TO-DIGITAL CONVERTER CIRCUIT
SE-905-TD	B	Granted	08/884787	30-Jun-1997	5994204	30-Nov-1999	SILICON GLASS-BONDED WAFERS
SE-1305-IP		Granted	08/883624	27-Jun-1997	5926384	20-Jul-1999	DC-DC CONVERTER HAVING DYNAMIC REGULATOR WITH CURRENT SOURCING AND SINKING MEANS
SE-1285-TD		Granted	08/885707	30-Jun-1997	5956583	21-Sep-1999	METHOD FOR FORMING COMPLIMENTARY WELLS AND SELF-ALIGNED TRENCH WITH A SINGLE MASK

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	FilDate	Patent	IssDate	Title
SE-1281-MS		Granted	08/748641	13-Nov-1996	5744984	28-Apr-1998	DRIVER CIRCUIT PROVIDING CONTROLLABLE BATTERY OVERLOAD PROTECTION
SE-1323-PD		Granted	08/885923	30-Jun-1997	6157076	05-Dec-2000	HERMETIC THIN PACK SEMICONDUCTOR DEVICE
SE-1161-IP		Granted	08/800421	14-Feb-1997	5808883	15-Sep-1998	DC-TO-DC CONVERTER HAVING CHARGE PUMP AND ASSOCIATED METHODS
SE-1364-DA		Granted	08/916569	22-Aug-1997	5949362	07-Sep-1999	DIGITAL-TO-ANALOG CONVERTER INCLUDING CURRENT CELL MATRIX WITH ENHANCED LINEARITY AND ASSOCIATED METHODS
SE-812	E	Granted	08/843302	14-Apr-1997	5801084	01-Sep-1998	BONDED WAFER PROCESSING
SE-1259-AP		Granted	08/918345	26-Aug-1997	5892375	06-Apr-1999	COMPARATOR WITH SMALL SIGNAL SUPPRESSION CIRCUITRY
SE-1259-AP	A	Granted	08/918307	22-Aug-1997	6060913	09-May-2000	COMPARATOR WITH SMALL SIGNAL SUPPRESSION CIRCUITRY
SE-1322-WR		Granted	08/941704	01-Oct-1997	5883565	16-Mar-1999	FREQUENCY DEPENDENT RESISTIVE ELEMENT
SE-1076-TL	A	Granted	08/873899	13-Jun-1997	5896053	20-Apr-1999	SINGLE ENDED TO DIFFERENTIAL CONVERTER AND 50% DUTY CYCLE SIGNAL GENERATOR AND METHOD
SE-1332-TD		Granted	08/964672	05-Nov-1997	5978192	02-Nov-1999	SCHMITT TRIGGER-CONFIGURED ESD PROTECTION CIRCUIT
SE-811	B	Granted	08/968618	12-Nov-1997	6051474	18-Apr-2000	NEGATIVE BIASING OF ISOLATION TRENCH FILL TO ATTRACT MOBILE POSITIVE IONS AWAY FROM BIPOLAR DEVICE REGIONS
SE-1192-TL		Granted	08/972887	18-Nov-1997	5977829	02-Nov-1999	LOW DISTORTION CURRENT FEEDBACK AMPLIFIER WITH DYNAMIC BIASING
SE-1286-TD		Granted	08/960337	29-Oct-1997	6034411	07-Mar-2000	INVERTED THIN FILM RESISTOR AND METHOD FOR MANUFACTURE
SE-1353-DA		Granted	09/006071	12-Jan-1998	6006071	21-Dec-1999	RF COMMUNICATIONS SYSTEM OPERABLE IN THE PRESENCE OF A REPETITIVE INTERFERENCE SOURCE AND RELATED METHODS

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	FilDate	Pat	IssDate	Title
SE-1268-MM		Granted	09/019241	05-Feb-1998	5990713	23-Nov-1999	ADJUSTABLE PHASE CLOCK CIRCUIT USING THE SAME AND RELATED METHODS
SE-1251-AP		Granted	09/024203	17-Feb-1998	5920224	06-Jul-1999	NETWORK FOR IMPROVING ELETRO-MAGNETIC INTERFERENCE RESPONSE
SE-1251-AP	A	Pending	09/024099	17-Feb-1998			NETWORK FOR IMPROVING ELETRO-MAGNETIC INTERFERENCE RESPONSE
SE-1283-TL		Granted	09/027257	20-Feb-1998	6167131	26-Dec-2000	RING GENERATOR
SE-826	A	Granted	08/956074	22-Oct-1997	5851864	22-Dec-1998	BICMOS DEVICES
SE-1250-TD	A	Granted	09/061602	16-Apr-1998	6130172	10-Oct-2000	RADIATION HARDENED DIELECTRIC FOR EEPROM
SE-800	B	Granted	09/378157	10-Mar-1998	6184565	06-Feb-2001	BIASING OF ISLAND-SURROUNDING MATERIAL TO SUPPRESS REDUCTION OF BREAKDOWN VOLTAGE DUE TO FIELD PLATE ACTING ON BURIED LAYER/ISLAND JUNCTION BETWEEN HIGH
SE-1367-AP		Granted	09/055528	06-Apr-1998	6069502	30-May-2000	SAMPLE-AND-HOLD CIRCUIT HAVING REDUCED SUBTHRESHOLD CONDUCTION EFFECTS AND RELATED METHODS
SE-1368-AP		Granted	09/055562	06-Apr-1998	6016067	18-Jan-2000	SAMPLE AND HOLD CIRCUIT HAVING REDUCED AMPLIFIER OFFSET EFFECTS AND RELATED METHODS
SE-1422-AP		Granted	09/055561	06-Apr-1998	6002277	14-Dec-1999	SAMPLE-AND-HOLD CIRCUIT HAVING REDUCED PARASITIC DIODE EFFECTS AND RELATED METHODS
SE-1373-TD		Granted	09/064029	21-Apr-1998	5932022	03-Aug-1999	SC-2 BASED PRE-THERMAL TREATMENT WAFER CLEANING PROCESS
SE-1327-PD		Granted	09/107475	30-Jun-1998	6159663	20-Dec-2000	METHOD OF CREATING A SOLDERABLE METAL LAYER ON GLASS OR CERAMIC
SE-1036-TD	A	Granted	09/073776	05-May-1998	5915168	22-Jun-1999	LID WAFER BOND PACKAGING AND MICROMACHINING
SE-1073-AP	A	Granted	08/854681	12-May-1997	6108352	22-Aug-2000	CIRCUIT AND METHOD FOR SYNCHRONIZING OUTPUTS OF TWO SIMULTANEOUSLY TRANSMITTING DEVICES IN A MULTIPLEXED COMMUNICATION SYSTEM

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Ap	FilDate	Pat	IssDate	Title
SE-1361-TL		Granted	09/079304	15-May-1998	6233335	15-May-2001	BATTERY SWITCHING SUBSCRIBER LOOP INTERFACE CIRCUIT
SE-1346-TD		Granted	09/082892	21-May-1998	5929508	27-Jul-1999	DEFECT GETTERING BY INDUCED STRESS
SE-1380-TD		Granted	09/106622	29-Jun-1998	6054012	25-Apr-2000	DECAPSULATING METHOD AND APPARATUS FOR INTEGRATED CIRCUIT PACKAGES
SE-1441-IP		Granted	09/108059	30-Jun-1998	6005303	21-Dec-1999	LINEAR VOLTAGE REGULATOR COMPATIBLE WITH BIPOLAR AND MOSFET PASS DEVICES AND ASSOCIATED METHODS
SE-1197-PD		Granted	09/109268	02-Jul-1998	6057612	02-May-2000	FLAT POWER PACK
SE-1277-TD		Granted	09/108963	02-Jul-1998	6064340	16-May-2000	ESD LOCATING APPARATUS AND METHOD
SE-1032-TD	A	Granted	09/110721	07-Jul-1998	6114768	05-Sep-2000	SURFACE MOUNT DIE BY HANDLE REPLACEMENT
SE-1053-TD	A	Granted	08/973769	27-Jul-1998	5973368	26-Oct-1999	HIGH EFFICIENCY POWER MOS SWITCH
SE-1429-TD	A	Granted	09/139932	26-Aug-1998	6278186	21-Aug-2001	PARASITIC CURRENT BARRIERS
SE-1406-DA		Granted	09/148955	08-Sep-1998	6107950	22-Aug-2000	ANALOG-TO-DIGITAL CONVERTER HAVING ENHANCED ACCURACY GAIN STAGE, AND ASSOCIATED DEVICES AND METHODS
SE-1439-DA		Granted	09/149154	08-Sep-1998	6118398	12-Sep-2000	DIGITAL-TO-ANALOG CONVERTER HAVING ENHANCED ACCURACY AND ASSOCIATED METHODS
SE-1442-TD		Granted	09/150429	09-Sep-1998	6140652	31-Oct-2000	DEVICE CONTAINING SAMPLE PREPARATION SITES FOR TRANSMISSION ELECTRON MICROSCOPIC ANALYSIS AND PROCESSES OF FORMATION AND USE
SE-1349-TL		Pending	09/145182	01-Sep-1998			PROGRAMMABLE SUBSCRIBER LOOP INTERFACE CIRCUIT AND METHOD
SE-1453-WR		Pending	09/163802	30-Sep-1998			PULSED BEACON-BASED INTERFERENCE REDUCTION MECHANISM FOR WIRELESS COMMUNICATION NETWORKS

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl#	FilDate	PatNum	IssDate	Title
SE-1374-IP		Granted	09/220780	24-Dec-1998	5982160	09-Nov-1999	DC-TO-DC CONVERTER WITH INDUCTOR CURRENT SENSING AND RELATED METHODS
SE-1024-TD	A	Granted	09/199292	24-Nov-1998	6211056	03-Apr-2001	INTEGRATED CIRCUIT AIR BRIDGE STRUCTURES AND METHOD OF FABRICATING SAME
SE-1472-TD		Granted	09/255231	22-Feb-1999	6255195	03-Jul-2001	BONDED SUBSTRATE FOR AN INTEGRATED CIRCUIT CONTAINING A PLANAR INTRINSIC GETTERING ZONE (as amended)
SE-1063-TD	A	Granted	09/204904	03-Dec-1998	6114191	05-Sep-2000	SEMICONDUCTOR PACKAGING APPARATUS
SE-1400-MM		Pending	09/245674	08-Feb-1999			METHOD OF DIGITALLY DECODING A COMPOSITE VIDEO SIGNAL AND A DIGITAL DECODER FOR COMPOSITE VIDEO SIGNALS
SE-1407-WR		Pending	09/231608	14-Jan-1999			METHOD OF PERFORMING ANTENNA DIVERSITY IN SPREAD SPECTRUM IN WIRELESS LOCAL AREA NETWORK
SE-1492-WR		Pending	09/231184	14-Jan-1999			WIRELESS LOCAL AREA NETWORK SPREAD SPECTRUM TRANSCEIVER WITH MULTIPATH MITIGATION
SE-1500-WR		Pending	09/231228	14-Jan-1999			SPREAD SPECTRUM TRANSCEIVER FOR USE IN WIRELESS LOCAL AREA NETWORK AND HAVING MULTIPATH MITIGATION
SE-1350-TL		Pending	09/208457	10-Dec-1998			APPARATUS AND METHOD FOR TESTING SUBSCRIBER LOOP INTERFACE CIRCUITS
SE-1322-WR	A	Granted	09/246815	09-Feb-1999	5999080	07-Dec-1999	FREQUENCY DEPENDENT RESISTIVE ELEMENT
SE-1094-LN	B	Granted	09/247510	10-Feb-1999	6114896	05-Sep-2000	COMPLEMENTARY MULTIPLEXER WITH LOW DISABLED-OUTPUT CAPACITANCE, AND METHOD
SE-1488-WR		Granted	09/261981	04-Mar-1999	6172556	09-Jan-2001	FEEDBACK-CONTROLLED LOW VOLTAGE CURRENT SINK/SOURCE
SE-1482-WR		Pending	09/266386	10-Mar-1999			SUCCESSIVE APPROXIMATION CORRECTION OF DC OFFSET IN FILTER-BUFFER BASEBAND PATH OF DATA RADIO
SE-1106-TD	A	Granted	09/268605	15-Mar-1999	6051457	18-Apr-2000	ELECTROSTATIC DISCHARGE PROTECTION DEVICE

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	ApNo	FiDate	PatNo	IssDate	Title
SE-1245-TD	A	Granted	09/266066	10-Mar-1999	6198150	06-Mar-2001	DEEP TRENCH ETCH ON BONDED SILICON WAFER
SE-1373-TD	A	Pending	09/335113	17-Jun-1999			SC-2 BASED PRE-THERMAL TREATMENT WAFER CLEANING PROCESS
SE-1176-MS	A	Granted	09/334998	17-Jun-1999	6233293	15-May-2001	CURRENT-CONTROLLED CARRIER TRACKING FILTER FOR IMPROVED SPURIOUS SIGNAL SUPPRESSION
SE-1278-TD	A	Pending	09/335134	17-Jun-1999			INTEGRATED CIRCUIT WITH THIN FILM RESISTORS AND A METHOD FOR CO-PATTERNING THIN FILM RESISTORS WITH DIFFERENT COMPOSITONS
SE-1346-TD	A	Granted	09/334987	17-Jun-1999	6274460	14-Aug-2001	DEFECT GETTERING BY INDUCED STRESS
SE-1479-WR		Granted	09/342583	29-Jun-1999	6233273	15-May-2001	RAKE RECEIVER WITH EMBEDDED DECISION FEEDBACK EQUALIZER
SE-1535-TD		Pending	09/345929	01-Jul-1999			LOW TEMPERATURE COEFFICIENT RESISTOR (TCRL)
SE-1371-TD		Pending	09/367325	11-Aug-1999			CO-PATTERNING THIN-FILM RESISTORS OF DIFFERENT COMPOSITIONS WITH A CONDUCTIVE HARD MASK AND METHOD FOR SAME
SE-1454-WR		Pending	09/378532	20-Aug-1999			PROGRAMMABLE FILTERING MECHANISM TO ALLOW BANDWIDTH OVERLAP BETWEEN DIRECT SEQUENCE SPREAD SPECTRUM COMMUNICATION DEVICE AND FREQUENCY-
SE-1348-TL		Pending	09/378962	23-Aug-1999			LOOP IMPEDANCE MEASURING APPARATUS AND METHOD FOR SUBSCRIBER LOOP INTERFACE CIRCUITS
SE-822-SP	G	Granted	09/394802	10-Sep-1999	6329260	11-Dec-2001	ANALOG-TO-DIGITAL CONVERTER AND METHOD OF FABRICATION
SE-1417-WR		Pending	09/426847	26-Oct-1999			TRANSCEIVER INCLUDING REACTIVE TERMINATION TO IMPROVE CROSS-MODULATION PERFORMANCE AND RELATED METHODS
SE-1380-TD	A	Pending	09/430391	29-Oct-1999			DECAPSULATING METHOD AND APPARATUS FOR INTEGRATED CIRCUIT PACKAGES
SE-1286-TD	A	Granted	09/429933	29-Oct-1997	6121105	19-Sep-2000	INVERTED THIN FILM RESISTOR AND METHOD FOR MANUFACTURE

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Client Ref	Sub Case	Status	Appl.	Fil Date	Pat.	Iss Date	Title
SE-1541-SP		Pending	09/442291	19-Nov-1999			BACKWARDS DRIVABLE MOS OUTPUT DRIVER
SE-1481-WR		Pending	09/494000	28-Jan-2000			BIASED-CORRECTED RAKE RECEIVER FOR DIRECT SEQUENCE SPREAD SPECTRUM WAVEFORM
SE-1562-TD		Pending	09/506711	18-Feb-2000			BREAKDOWN IMPROVEMENT METHOD AND STRUCTURE FOR LATERAL EXTENSION MOS DEVICE
SE-1393-IP	A	Granted	08/974862	20-Nov-1997	6058030	02-May-2000	MULTIPLE OUTPUT DC-TO-DC CONVERTER HAVING ENHANCED NOISE MARGIN AND RELATED METHODS
SE-1375-PD	A	Granted	09/030871	19-May-2000	6275093	14-Aug-2001	IGBT GATE DRIVE CIRCUIT WITH SHORT CIRCUIT PROTECTION
SE-1541-SP	A	Pending	09/569894	12-May-2000			BACKWARDS DRIVABLE MOS OUTPUT DRIVER
SE-1539-IP		Granted	09/591404	12-Jun-2000	6278263	21-Aug-2001	MULTI-PHASE CONVERTER WITH BALANCED CURRENTS
SE-1536-IP		Granted	09/591360	09-Jun-2000	6181120	30-Jan-2001	CURRENT MODE DC/DC CONVERTER WITH CONTROLLED OUTPUT IMPEDANCE
SE-1489-WR		Pending	09/571822	16-May-2000			AN ULTRA LINEAR HIGH FREQUENCY TRANSCONDUCTOR STRUCTURE
SE-1616-WR		Pending	09/586571	02-Jun-2000			A DUAL PACKET CONFIGURATION FOR WIRELESS COMMUNICATIONS
SE-1388-DA		Pending	09/524992	14-Mar-2000			SUBSAMPLING DIGITIZER-BASED FREQUENCY SYNTHESIZER
SE-1535-TD	A	Pending	09/607080	29-Jun-2000			LOW TEMPERATURE COEFFICIENT RESISTOR (TCRL)
SE-1323-PD	A	Pending	09/621449	21-Jul-2000			HERMETIC THIN PACK SEMICONDUCTOR DEVICE
SE-1519-WR		Pending	09/572417	17-May-2000			APPARATUS FOR RADIO FREQUENCY PROCESSING WITH SINGLE OSCILLATOR FOR INTERMEDIATE FREQUENCY PROCESSING

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl#	FilDate	Pat#	IssDate	Title
SE-1520-WR		Pending	09/573782	17-May-2000			APPARATUS FOR RADIO FREQUENCY PROCESSING WITH DUAL MODULUS SYNTHESIZER
SE-1537-IP		Granted	09/633316	07-Aug-2000	6246220	12-Jun-2001	SYNCHRONOUS-RECTIFIED DC TO DC CONVERTER WITH IMPROVED CURRENT SENSING AND ASSOCIATED METHODS
SE-1510-WR		Pending	09/612848	10-Jul-2000			NEGATIVE FEEDBACK GAIN CONTROL FOR COMMON ELECTRODE TRANSISTOR
SE-1597-IP		Pending	09/639407	14-Aug-2000			OSCILLATOR HAVING REDUCED SENSITIVITY TO SUPPLY VOLTAGE CHANGES
SE-1480-WR		Pending	09/612823	10-Jul-2000			RAPID ESTIMATION OF WIRELESS CHANNEL IMPULSE RESPONSE
SE-1573-TL		Pending	09/639408	14-Aug-2000			TRANSCONDUCTANCE AMPLIFIER CIRCUIT
SE-1598-IP		Granted	09/645070	23-Aug-2000	6249446	19-Jun-2001	CASCADABLE, HIGH EFFICIENCY CHARGE PUMP CIRCUIT AND RELATED METHODS
SE-1563-TL		Pending	09/686505	11-Oct-2001			PRECISION, LOW-POWER CURRENT-SENSE TRANSMISSION CHANNEL FOR SUBSCRIBER LINE INTERFACE CIRCUIT, PROGRAMMABLE WITH SINGLE ENDED IMPEDANCES AND CAPABLE OF
SE-1584-TL		Pending	09/686926	11-Oct-2000			BIASING ARRANGEMENT FOR OPTIMIZING DC FEED CHARACTERISITICS FOR SUBSCRIBER LINE INTERFACE CIRCUIT
SE-1564-TL		Pending	09/686504	11-Oct-2000			MECHANISM FOR PREVENTING CLIPPING OF PULSE METERING SIGNALS IN TELEPHONE LINE CARD CHANNELS
SE-1579-TL		Pending	09/686247	11-Oct-2000			CONTROLLED SWITCHING MECHANISM FOR ACCOMPLISHING SOFT POLARITY REVERSAL, RING-TRIP FILTERING, AND LINE VOLTAGE MEASUREMENTS IN A SUBSCRIBER LINE
SE-1572-TL		Pending	09/686514	11-Oct-2000			MECHANISM FOR MINIMIZING UNDESIRABLE EFFECTS OF PARASITIC COMPONENTS IN INTEGRATED CIRCUITS
SE-1568-TL		Pending	09/686515	11-Oct-2000			MECHANISM FOR GENERATING PRECISION USER-PROGRAMMABLE PARAMETERS IN ANALOG INTEGRATED CIRCUIT
SE-1567-TL		Pending	09/686517	11-Oct-2000			MECHANISM FOR MEASURING RESISTANCE OF TELEPHONE SUBSCRIBER LINE AND GENERATING MEASUREMENT AS PULSE WIDTH OF PERIODIC WAVEFORM

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	SubCase	Status	Appl	FiDate	Pat	IssDate	Title
SE-1581-TL		Pending	09/686634	11-Oct-2000			TRANSISTOR BASE CURRENT ERROR CORRECTION SCHEME FOR LOW OVERHEAD VOLTAGE APPLICATIONS
SE-1577-TL		Pending	09/686633	11-Oct-2000			CURRENT MIRROR-EMBEDDED LOW-PASS FILTER FOR SUBSCRIBER LINE INTERFACE CIRCUIT APPLICATIONS
SE-1569-TL		Granted	09/686506	11-Oct-2000	6292033	18-Sep-2001	PRECISION, LOW-POWER TRANSIMPEDANCE CIRCUIT WITH DIFFERENTIAL CURRENT SENSE INPUTS AND SINGLE ENDED VOLTAGE OUTPUT
SE-1666-WR		Pending	09/252308	11-Feb-1999			DATA COMMUNICATON NETWORK
SE-1667-WR		Pending	09/527407	17-Mar-2000			INTERFACE CARD
SE-1668-WR		Pending	09/526607	16-Mar-2000			PROTECTED DATA TRAFFIC
SE-1621-WR		Pending	09/678901	02-Oct-2000			DC COMPENSATION SYSTEM FOR A WIRELESS COMMUNICATION DEVICE CONFIGURED IN A ZERO INTERMEDIATE FREQUENCY ARCHITECTURE
SE713	A	Pending	09/570009	12-May-2000			VARIABLE WAVELENGTH OPTICAL ALIGN SYSTEM
SE-1588-WR		Pending	09/717459	20-Nov-2000			DUAL-EDGE FUNCTION CLOCK GENERATOR AND METHOD OF DERIVING CLOCKING SIGNALS FOR EXECUTION REDUCED INSTRUCTION SEQUENCES IN A RE-PROGRAMMABLE I/O INTERFACE
SE-1589-WR		Pending	09/717495	20-Nov-2000			SEQUENCER AND METHOD OF SELECTIVELY INHIBITING CLOCK SIGNALS TO EXECUTE REDUCED INSTRUCTION SEQUENCES IN A RE-PROGRAMMING I/0 INTERFACE
SE-1641-WR		Pending	09/747138	21-Dec-2000			SYSTEM AND METHOD FOR DETECTING AND CORRECTING PHASE ERROR BETWEEN DIFFERENTIAL SIGNALS
SE-1630-WR		Pending	09/747321	21-Dec-2000			BIAS CIRCUIT FOR A LOW VOLTAGE DIFFERENTIAL CIRCUIT
SE-1631-WR		Pending	09/747163	21-Dec-2000			QUADRATURE OSCILLATOR WITH PHASE ERROR CORRECTION
SE-1576-TL		Pending	09/686324	11-Oct-2000			PRECISION LOOP VOLTAGE DETECTOR FOR SUBSCRIBER LINE INTERFACE CIRCUIT APPLICATIONS

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Client Ref	SubCase	Status	Appl	Fil Date	Pat	Iss Date	Title
SE-1622-WR		Pending	09/677975	02-Oct-2000			A CALIBRATED DC COMPENSATION SYSTEM FOR A WIRELESS COMMUNICATION DEVICE CONFIGURED IN A ZERO INTERMEDIATE FREQUENCY ARCHITECTURE
SE-1629-WR		Pending	60/259295	02-Jan-2001			PRECISION PROGRAMMABLE WIDEBAND AUTOMATIC GAIN CONTROL AMPLIFIER
SE-1560-MS		Pending	09/741221	19-Dec-2000			OVERVOLTAGE PROTECTION CIRCUIT FOR BIDIRECTIONAL TRANSMISSION GATE
SE-1632-WR		Pending	09/746736	21-Dec-2000			A SWITCHED ELECTROSTATIC DISCHARGE RING FOR INTEGRATED CIRCUITS WITH MULTIPLE POWER INPUTS
SE-1558-IP		Pending	09/791509	22-Feb-2001			METHODS TO CONTROL THE DROOP WHEN POWERING DUAL MODE PROCESSORS AND ASSOCIATED CIRCUITS
SE-1596-WR		Pending	60/274261	08-Mar-2001			INTEROPERABLE FORWARD ERROR CORRECTION IN A NETWORK WITH HETEROGENEOUS STATION CAPABILITIES
SE-1731-TD		Pending	60/282011	06-Apr-2001			DESIGN OF AN ON-WAFER TEST STRUCTURE TO DETECT PROCESS-INDUCED HIGH FREQUENCY PARAMETRIC VARIATIONS THROUGH DC MEASUREMENTS
SE-1517-PD	B	Pending	09/815672	23-Mar-2001			EDGE TERMINATION FOR SILICON POWER DEVICES
SE-1479-WR	A	Pending	09/823845	30-Mar-2001			RAKE RECEIVER WITH EMBEDDED DECISION FEEDBACK EQUALIZER
SE-1472-TD	A	Pending	09/846795	01-May-2001			BONDED SUBSTRATE FOR AN INTEGRATED CIRCUIT CONTAINING A PLANAR INTRINSIC GETTERING ZONE (as amended)
SE-1602-IP		Pending	09/846721	01-May-2001			DC TO DC CONVERTER METHOD AND CIRCUITRY
SE-1176-MS	B	Pending	09/855332	15-May-2001			CURRENT-CONTROLLED CARRIER TRACKING FILTER FOR IMPROVED SPURIOUS SIGNAL SUPPRESSION
SE-1696-WR	P	Pending	60/272187	28-Feb-2001			AN AUTOMATIC GAIN CONTROL CIRCUIT WITH HIGH LINEARITY AND MONOTONICALLY CORRELATED OFFSET VOLTAGE
SE-1620-WR		Pending	09/849002	04-May-2001			A SYSTEM AND METHOD OF REPETITIVE TRANSMISSION OF FRAMES FOR FRAME-BASED COMMUNICATIONS

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

ClientRef	Subcase	Status	Appl	Filed Date	Patent	Issue Date	Title
SE-1618-WR		Pending	09/849053	04-May-2001			SYSTEM AND METHOD FOR SYNCHRONIZING DATA TRANSMISSION ACROSS AN INTERFACE WITH VARIABLE TIMING
SE-1619-WR		Pending	09/849101	04-May-2001			A SYSTEM AND METHOD FOR PROVIDING A SELECTABLE RETRY STRATEGY FOR FRAME-BASED COMMUNICATIONS
SE-1614-WR	O	Pending	09/864676	24-May-2001			A COMMUNICATION SYSTEM USING ORTHOGONAL WAVELET DIVISION MULTIPLEXING (OWDM) AND OWDM-SPREAD SPECTRUM (OWSS) SIGNALING
SE-1385-TD	A	Pending	09/062964	23-May-2001			DEVICE WITH AND METHODS FOR PATTERNED WELLS
SE-1468-TD	A	Pending	09/961613	24-Sep-2001			METHOD FOR MAKING A DIFFUSED BACK-SIDE LAYER ON A BONDED-WAFER WITH A THICK BOND OXIDE
SE-1661-MS	O	Pending	09/973106	09-Oct-2001			REDUNDANT COMPARATOR DESIGN FOR IMPROVED OFFSET VOLTAGE AND SINGLE EVENT EFFECTS HARDNESS
SE-822-SP	H	Pending	09/973390	09-Oct-2001			ANALOG-TO-DIGITAL CONVERTER AND METHOD OF FABRICATION
SE-1660-TD		Pending		12-Oct-2001			INTEGRATED CIRCUIT WITH A MOS STRUCTURE HAVING REDUCED PARASITIC BIPOLAR TRANSISTOR ACTION
SE-1555-MS	O	Pending		30-Oct-2001			REDUNDANT LATCH CIRCUIT AND ASSOCIATED METHODS
SE-1301-WR	a	Pending	982807	09-Nov-2001			HIGH DATA RATE SPREAD SPECTRUM TRANSCEIVER AND ASSOCIATED METHODS
SE-1540-TD		Pending		21-Nov-2001			SELF-ALIGNMENT OF SEPARATED REGIONS IN A LATERAL MOSFET STRUCTURE OF AN INTEGRATED CIRCUIT
SE-1712-MS	O	Pending	09/996448	28-Nov-2001			SPATIALLY REDUNDANT AND COMPLEMENTARY SEMICONDUCTOR DEVICE-BASED, SINGLE EVENT TRANSIENT-RESISTANT LINEAR AMPLIFIER CIRCUIT ARCHITECTURE
SE-1211-TD	c	Pending		16-Nov-2001			WAFER TRENCH ARTICLE AND PROCESS
SE-1669-WR	o	Pending	10/005096	03-Dec-2001			COMMON MODE OUTPUT CURRENT CONTROL CIRCUIT AND METHOD

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

OurRefNo	SubCase	Status	AppNo	FilDate	PatNo	IssDate	Title
SE-1642-WR	O	Pending		03-Dec-2001			ATTENUATOR CONTROL CIRCUIT
SE-1735-WR		Pending	09/943803	31-Aug-2001			SYSTEM AND METHOD FOR ORDERING DATA MESSAGES HAVING DIFFERING LEVELS OF PRIORITY FOR TRANSMISSION OVER A SHARED COMMUNICATION CHANNEL
SE-1463-TD	A	Pending	09/949736	10-Sep-2001			LASER DECAPSULATION APPARATUS AND METHOD
SE-1730-IP	O	Pending	09/950469	10-Sep-2001			METHOD TO SET OUTPUT VOLTAGE OF INTEGRATED PWM CONTROLLER AND A CIRCUIT FOR THEREOF
SE-1633-WR		Pending	09/952184	14-Sep-2001			LINEARIZATION BIAS CIRCUIT FOR BJT AMPLIFIERS
SE-1647-TD		Pending	09/877272	08-Jun-2001			LATERAL DMOS STRUCTURE WITH LATERAL EXTENSION STRUCTURE FOR REDUCED CHARGE TRAPPING IN GATE OXIDE
SE-1451-TD		Pending	09/880726	13-Jun-2001			REFERENCE CURRENT/VOLTAGE GENERATOR HAVING REDUCED SENSITIVITY TO VARIATIONS IN POWER SUPPLY VOLTAGE
SE-1734-BW		Pending	09/884000	19-Jun-2001			REMOTE POWER AMPLIFIER LINEARIZATION
SE-1663-DA	O	Pending	09/900588	06-Jul-2001			AN OPERATIONAL AMPLIFIER INCLUDING A RIGHT-HALF PLANE ZERO REDUCTION CIRCUIT AND RELATED METHOD
SE-1741-WR		Pending	60/303444	06-Jul-2001			MIXED WAVEFORM CONFIGURATION FOR WIRELESS COMMUNICATIONS
SE-1574-TL		Pending	09/901259	09-Jul-2001			MULTISTAGE PRECISION, LOW INPUT/OUTPUT OVERHEAD, LOW POWER, HIGH OUTPUT IMPEDANCE AND LOW CROSSTALK CURRENT MIRROR
SE-1575-TL		Pending	09/901439	09-Jul-2001			MECHANISM FOR MINIMIZING CURRENT MIRROR TRANSISTOR BASE CURRENT ERROR FOR LOW OVERHEAD VOLTAGE APPLICATIONS
SE-1570-TL		Pending	09/901265	09-Jul-2001			PRECISION LOW POWER OPERATIONAL AMPLIFIER WITH GAIN INVARIANT BANDWIDTH
SE-1585-TL		Pending	09/901260	09-Jul-2001			TRANSCONDUCTANCE AMPLIFIER BASED PRECISION HALF WAVE AND FULL WAVE RECTIFIER CIRCUIT

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Client Ref	Subcase	Status	App/Ap	Filing Date	Pat	Iss Date	Title
SE-1582-TL		Pending	09/901327	09-Jul-2001			REDUCED PROPAGATION DELAY CURRENT MODE CASCADED ANALOG-TO-DIGITAL CONVERTER AND THRESHOLD BIT CELL THEREFOR
SE-1565-TL		Pending	09/901326	09-Jul-2001			TEMPERATURE-INSENSITIVE OUTPUT CURRENT LIMITER NETWORK FOR ANALOG INTEGRATED CIRCUIT
SE-1689-TD		Pending	09/899332	03-Jul-2001			MOSINTEGRATED CIRCUIT WITH REDUCED ON RESISTANCE
SE-1698-TL	O	Pending	09/909183	19-Jul-2001			SUBSCRIBER LINE INTERFACE CIRCUIT (SLIC) INCLUDING A TRANSIENT OUTPUT CURRENT LIMIT CIRCUIT AND RELATED METHOD
SE-1578-TL		Pending	09/901506	09-Jul-2001			CAPACITOR MULTIPLIER
SE-1664-WR	O	Pending	09/911060	23-Jul-2001			MIXER DRIVER CIRCUIT
SE-1554-MS	O	Pending	09/915119	25-Jul-2001			POWER DEVICE DRIVING CIRCUIT AND ASSOCIATED METHODS
SE-1623-WR	o	Pending	09/918409	30-Jul-2001			PACKET ACQUISITION AND CHANNEL TRACKING FOR A WIRELESS COMMUNICATION DEVICE CONFIGURED IN A ZERO INTERMEDIATE FREQUENCY ARCHITECTURE
SE-1553-MS	O	Pending	09/918208	30-Jul-2001			COMPLEMENTARY METAL OXIDE SEMICONDUCTOR WITH IMPROVED SINGLE EVENT PERFORMANCE
SE-1211-TD	B	Pending	283530	26-Jul-2001			WAFER TRENCH ARTICLE AND PROCESS
SE-1652-IP	O	Pending	09/928857	13-Aug-2001			INTEGRATED CIRCUIT WITH CURRENT-LIMITED POWER OUTPUT AND ASSOCIATED METHOD
SE-1653-IP	O	Pending	09/928821	13-Aug-2001			INTEGRATED CIRCUIT WITH CURRENT SENSE CIRCUIT
SE-1738-SP	O	Pending	60/293445	21-Aug-2001			APPARATUS AND METHOD FOR MINIMIZING SPURIOUS HARMONIC NOISE IN SWITCHED CURRENT STEERING ARCHITECTURES
SE-1569-TL	a	Pending	09/939191	24-Aug-2001			PRECISION, LOW-POWER TRANSIMPEDANCE CIRCUIT WITH DIFFERENTIAL CURRENT SENSE INPUTS AND SINGLE ENDED VOLTAGE OUTPUT

SCHEDULE A
(i) PATENTS AND PATENT APPLICATIONS

Client Ref	SubCase	Status	Appl	Appl Date	Patt	Iss Date	Title
SE-1659-WR	O	Pending	09/943668	31-Aug-2001			A VARIABLE TRANSCONDUCTANCE AMPLIFIER
SE-1673-WR	o	Pending	09/944000	31-Aug-2001			SINGLE-ENDED TO DIFFERENTIAL AND DIFFERENTIAL TO SINGLE-ENDED CONVERSION USING A COMMON MODE SHUNT
28-IS-0064		Granted	07/740700	06-Aug-1991	5184128	02-Feb-1993	INTEGRATING A/D CONVERTER WITH MEANS FOR REDUCING ROLLOVER ERROR
XRCA78203		Granted	817489	09-Jan-1986	4882749	21-Nov-1989	CONTROL OF SIGNAL TRANSMISSION
XRCA78673		Granted	220712	18-Jul-1988	4924113	08-May-1990	TRANSISTOR BASE CURRENT COMPENSATION CIRCUITRY
XRCA79485		Granted	605241	30-Apr-1984	4594517	10-Jun-1986	POWER DOWN SENSOR
XRCA83734		Granted	915985	03-Oct-1986	4785339	15-Nov-1988	INTEGRATED LATERAL PNP TRANSISTOR AND CURRENT LIMI
RD 15280		Granted	530328	08-Sep-1983	4472628	18-Sep-1984	FIBER OPTICS TRANSDUCER FOR SENSING PARAMETER MAGNITUDE
XRCA79243		Granted	695297	28-Jan-1985	4730131	08-Mar-1988	INPUT SIGNAL CONDITIONING CIRCUIT

SCHEDULE A
PATENT DISCLOSURES

Client Ref. #	Disclosure Status	Invention
SE-1625-WR	Authorized	ZIF ARCHITECTURE WITH MULTIPLEXED AUTOMATIC GAIN CONTROL AMPLIFIER
SE-1766-WR	Authorized	THRESHOLD DETECTION OF CORRELATOR OUTPUT FOR OFDM ACQUISITION
SE-1769-IP	Authorized	METHOD OF SETTING AND DETECTING FAST LOOP TRIP POINTS
SE-1514-TD	Authorized	CAPACITIVE COUPLED LEVEL SHIFTER AND METHOD
SE-1545-TD	Authorized	ESD PROTECTION NETWORKS UTILIZING PRECHARGED BUS LINES
SE-1591-WR	Authorized	PROGRAMMABLE INTERFACE APPARATUS HAVING INSTRUCTION WITH CONDITIONAL EXECUTION DURATION
SE-1592-WR	Authorized	PROGRAMMABLE INTERFACE APPARATUS HAVING LOOP CONTROL INSTRUCTION WITH DATA-DEPENDENT OVERRIDE
SE-1593-WR	Authorized	PROGRAMMABLE INTERFACE APPARATUS HAVING A PROGRAM COUNTER THAT OPERATES AS A BIT COUNTER
SE-1759-BW	Authorized	CONNECTIONLESS COMMUNICATION NETWORK AND WIRELESS CHANNEL ALLOCATION METHOD THEREFOR
SE-1626-WR	Authorized	ANTENNA DIVERSITY
SE-1627-WR	Authorized	FORWARD ERROR CORRECTION SCHEME
SE-1628-WR	Authorized	APRIORI FREQUENCY OFFSET
SE-1636-WR	Authorized	VOLTAGE CONTROLLED OSCILLATOR (VCO)
SE-1733-TD	Authorized	ENHANCED EPROM STRUCTURES AND METHOD OF FABRICATION
SE-1726-SP	Authorized	AN ANALOG TO DIGITAL CONVERTER WITH INTERPOLATING AND SUBRANGING ARCHITECTURE
SE-1727-SP	Authorized	DIFFERENTIAL CALIBRATION OF RESISTIVE LADDER USING PARALLEL RESISTIVE CORRECTION
SE-1728-SP	Authorized	DIFFERENTIAL CALIBRATION OF PREAMPLIFIER OFFSETS
SE-1729-SP	Authorized	HIGH SPEED TRACK AND HOLD CIRCUIT WITH DUAL PUMP CIRCUIT

SCHEDULE A
PATENT DISCLOSURES

Client Ref. #	Disclosure Status	Inv. Title
SE-1732-TD	Authorized	PATTERNED GROUND SHIELDS AND OTHER LAYOUT INNOVATIONS FOR SYMMETRIC ON-CHIP TRANSFORMERS
SE-1748-WR	Authorized	A RAPID ACQUISITION AND TRACKING SYSTEM FOR A WIRELESS PACKET BASED COMMUNICATION DEVICE
SE-1640-WR	Authorized	AUTOMATIC PER CHANNEL POWER SETTING AND PROGRAMMING BASED ON SIDELOBE LEVEL
SE-1746-WR	Authorized	MAGNETIC THIN FILM INDUCTORS
SE-1747-TL	Authorized	IMPROVED EFFICIENCY EL-DRIVER
SE-1772-IP	Open	SYNTHETIC RIPPLE REGULATOR
SE-1770-BW	Open	POWER AMPLIFIER MEMORY-EFFECT COMPENSATION WITH INTERPOLATED PRESDISTORTION
SE-1773-IP	Open	AUTOMATIC DEADTIME ADJUSTMENT FOR DC TO DC POWER DRIVER
SE-1764-TL	Open	A LINE VOLTAGE REGULATOR CIRCUIT FOR SUBSCRIBER LINE APPLICATIONS
	Open	
SE-1763-TL	Open	A HIGH VOLTAGE INTERFACE CIRCUIT FOR SUBSCRIBER LINE APPLICATIONS
SE-1750-TD	Open	REDUCED MASK COUNT DUAL BURIED LAYER PROCESS
SE-1774-IP	Open	AUTO-ZEROED VIRTUAL GROUND CURRENT SENSE TECHNIQUE FOR DC TO DC CONVERTER DRIVER
SE-1775-IP	Open	CONTROLLED TURN ON OF UPPER FET TO CONTROL PHASE RINGING IN BUCK PWM DC TO DC
SE-1776-IP	Open	LEVEL SHIFTED LOWER GATE DRIVER FOR DC TO DC DRIVER
SE-1611-WR	Open	IMPROVED FEC REPEAT CODE DEMODULATION METHOD
SE-1781-IP	Open	TECHNIQUE TO PREVENT CURRENT INJECTION INTO UPPER FET OF SYNCHRONOUS BUCK DC TO DC
SE-1740-TL	Open	CIRCUIT DESIGN FOR TESTING HIGH PERFORMANCE DEVICES

SCHEDULE A
PATENT DISCLOSURES

Client Ref	Disclosure Status	Invention
SE-1658-SP	Open	SINGLE BIT OVER-SAMPLED A/D - D/A SERVE CONTROL OF LOAD CURRENT IN A POWER MOSPET
SE-1780-IP	Open	TECHNIQUE TO USE "PILOTED" LOWER N-CHANNEL FET FOR CURRENT SENSING IN PWM APPLICATIONS